

LogicPak™

Maintenance Manual

DATA I/O



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303A LOGICPAK™

Maintenance Manual

972-0142-003

August 87

Data I/O Corporation warrants to the original purchaser of the product described by this manual that the product was fully functional to the extent of its specification at the time of shipment from the factory. Data I/O further certifies that the equipment used to test the product was calibrated to standards that are traceable to the National Bureau of Standards as appropriate.

ORDERING INFORMATION

When ordering this manual, use Part Number 972-0142-003.
Applies to: Engineering Part No. 950-1942-008 and up.

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SAFETY SUMMARY

General safety information for operating personnel is contained in this summary. In addition, specific WARNINGS and CAUTIONS appear throughout this manual where they apply and are not included in this summary.

DEFINITIONS

WARNING statements identify conditions or practices that could result in personnel injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to equipment or other property.

SYMBOLS

V ~ This symbol stands for Vac. For example, 120 ~ = 120 Vac.

GROUNDING THE PRODUCT

The product is grounded through the grounding conductor of the power cord. To avoid electric shock, plug the power cord into a properly wired and grounded receptacle only. Grounding this equipment is essential for safe operation.

POWER CORD

Use only the power cord specified for your equipment.

SERVICING

To reduce the risk of electric shock, do not perform any servicing other than that described in this manual.

FUSE REPLACEMENT

For continued protection against the possibility of fire, replace only with a fuse of the specified voltage, current and type ratings.

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1. INTRODUCTION

1.1 GENERAL

This manual contains maintenance information specific to the LogicPak and the associated P/T (programming and testing) adapters. This manual is divided into the following major areas:

- **INTRODUCTION** — Provides descriptive information for the LogicPak and associated P/T adapters. Also contains warranty, ordering, and service information.
- **INSTALLATION** — Describes the installation of the LogicPak into the programmer and of the P/T adapter into the LogicPak.
- **CIRCUIT DESCRIPTION** — Describes the theory of operation for the LogicPak and associated P/T adapters.
- **MAINTENANCE** — Describes cleaning and physical inspection of the LogicPak.
- **CALIBRATION** — Describes the periodic or post-repair calibration of the LogicPak with reference to Appendix A.
- **TROUBLESHOOTING** — Describes fault isolation of the unit.
- **APPENDIX A** — Contains calibration measurement charts and calibration timing diagrams for the LogicPak.
- **APPENDIX B** — Contains a complete set of schematic diagrams of the LogicPak and P/T adapters.

1.2 LOGICPAK OVERVIEW

The Data I/O LogicPak configures Data I/O programmers to program and test a variety of logic devices in engineering and production environments. The LogicPak accepts all Data I/O P/T adapters as well as PALASM and H&L Design Adapters.

NOTE

This manual covers the LogicPak and all P/T adapters. For information on the PALASM and H&L Design Adapters, refer to the respective manual supplied with the adapter.

Like other Data I/O programming paks, the LogicPak is designed to interface with a standard programmer such as the Model 29 Universal Programmer (see subsection 1.3 for programmer compatibility) to form a programmable logic development system. The LogicPak contains all necessary firmware and electronics to control the flow of data to and from the user, as well as throughout the system. In this manual we will refer to the operational procedures for the Model 29 Universal Programmer; refer to your programmer manual for System 19 and 100A production programmer key sequences.

When a P/T adapter is installed in the LogicPak, and the LogicPak is installed in the Model 29 programmer, the programmer can program the logic devices specific to that P/T adapter. The LogicPak receives its power from the programmer power supplies. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the LogicPak.

1.3 PROGRAMMER COMPATIBILITY

In addition to the Model 29, Data I/O's System 19 Universal Programmer and 100A Production Programmer are compatible with the LogicPak. To be compatible with the LogicPak, your programmer may require a hardware and/or firmware update, depending on the model, configuration, and age. The following information will help you determine whether your programmer requires updating. If you find that your programmer does require updating, contact your nearest Data I/O service center. (Call (800)-247-5700 for the number of your local service center.)

Table 1-1A shows whether your programmer requires an update to be compatible with the LogicPak. Table 1-1B shows which programmer can operate with each P/T adapter.

- System 17 — The System 17 must be converted into a System 19 with the latest firmware installed and with the latest hardware modifications.
- System 19 — Check to determine whether your System 19 contains a 702-1520 or 702-1980 controller board by performing the following steps:
 1. Remove the programming pak.
 2. Remove the metal shield (if any, see subsection 2.2, figure 2-1).
 3. Count the number of EPROM firmware sockets located just behind the pak interface connector. If there are four sockets, it is a 702-1520 board. If there are eight sockets, it is a 702-1980 board.

If your System 19 contains a 702-1520 controller board, check the modification status sticker on the bottom of the programmer. If the sticker is not there, or if the 1 is marked, your System 19 requires hardware and firmware updating. Contact the nearest Data I/O service center. If 2 is marked, your System 19 is compatible with the LogicPak. If your System 19 contains a 702-1980 controller board, it may require a firmware update. To display the configuration number of the firmware in your programmer, press SELECT, B, 2, and START. If the configuration number displayed is 3599 or CC8B, your firmware needs updating.

- **Model 29 Universal Programmer** — To be compatible with the LogicPak, the Model 29 programmers must have Rev (revision) C or later firmware. To determine the configuration of the firmware in your Model 29, press SELECT, B, 2, and START, then observe the display. If the hexadecimal number matches one listed in table 1-1, your firmware needs to be updated.
- **100A Production Programmer** — To be compatible with the LogicPak, the 100A programmers must have Rev E or later firmware. To determine the configuration of the firmware in your 100A, press SELECT, 1, 0, and START, then observe the display. If the hexadecimal number display matches one listed in table 1-1, your firmware needs to be updated.

Table 1-1A. Programmer Update Configurations

Model	Revision	Configuration Number
29A	A	1ECA
	B	20A4
29A (with computer remote control)	A	BB41
	B	C00B
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

Table 1-1B. P/T Adapter Compatibility Table

P/T Adapter	Programmer	Minimum Programmer RAM
303A-001	29A, 29B, System 19, Model 100A	8K
303A-007	29A, 29B, System 19, Model 100A	8K
303A-008A/B	29A, 29B	64K
303A-010	29A, 29B	64K
303A-011A	29A, 29B, System 19	16K
303A-011B	29A, 29B, System 19	16K
303A-012	29A, 29B, System 19	16K

Check for additional programmer compatibility requirements in the LogicPak Operator's manual and your P/T adapter User Note.

1.4 SPECIFICATIONS

The physical and environmental specifications of the LogicPak are:

- Altitude (operating): sea level to 3 km (10,000 ft)
- Humidity (operating): 90% maximum (noncondensing)
- Temperature (operating): 5 to 45°C (41 to 113°F)
- Temperature(storage): -40 to 70°C (-40 to 158°F)
- Weight: 2.2 kg (4 lb, 12 oz)
- Dimensions: 24.13 x 17.02 x 14.48 cm (9.5 x 6.7 x 5.7 in.)

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has field applications engineers throughout the world. They can provide additional information about interfacing Data I/O products with other systems and answer questions about your equipment. Please call one of the numbers listed below for the number of your local service center:

In the U.S.: (800) 247-5700
(except for Washington State, call (206) 881-6444
Data I/O Canada: (416) 678-0761
Data I/O Europe: 011-31-20-622-866
Data I/O Japan: 011-81-3-432-6991
All other locations: (206) 881-6444

1.6 WARRANTY

The Data I/O LogicPak is warranted against defects in materials and workmanship. The warranty period of one year begins when you receive the equipment; the warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but also calibration of all Data I/O products. Please call one of the numbers listed above for the number of your local service center.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative. Orders for shipment must include:

- a description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- purchase order number
- desired method of shipment
- quantity of each item ordered
- shipping and billing address of the firm, including ZIP code
- name of person ordering the equipment.

2. INSTALLATION

2.1 LOGICPAK INSTALLATION

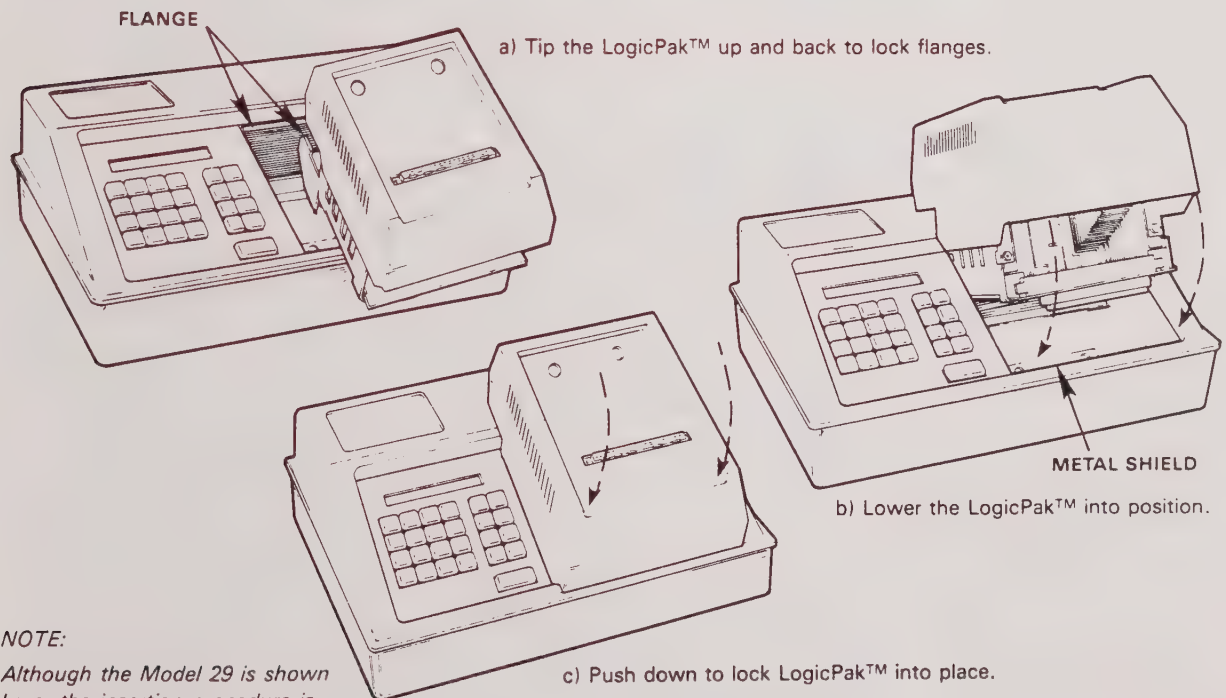
The LogicPak may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the LogicPak is installed, you will hear a beep until the LogicPak with an adapter is installed.

CAUTION

Voltage transients can cause device damage. If a P/T (programming/testing) adapter is installed in the LogicPak, be sure that all sockets are empty when switching power on or off, or installing or removing the LogicPak or adapter.

To install the LogicPak, proceed as follows:

1. Slide the LogicPak into the opening in the programmer (see figure 2-1a).



NOTE:

Although the Model 29 is shown here, the insertion procedure is the same for all systems.

Figure 2-1. LogicPak Installation

2. Tilt the LogicPak up and gently push it back to hook the flange of the LogicPak over the back edge of the programmer opening (see figure 2-1a).
3. Lower the LogicPak into position (see figure 2-1b).
4. Press gently on the front edge of the LogicPak to ensure a good connection (see figure 2-1c).

2.2 ADAPTER INSTALLATION

To insert an adapter in the LogicPak, proceed as follows:

1. Check to make sure a device is not in a socket. If a device is in a socket, remove it.
2. Align the guide pins on the underside of the adapter with the guide pin holes on the LogicPak (see figure 2-2).
3. Gently set the adapter on the LogicPak. Make sure the guide pins line up with the guide pin holes.
4. Firmly press down on the front edge of the adapter to lock the connector pins into the connector receptacle (see figure 2-2).

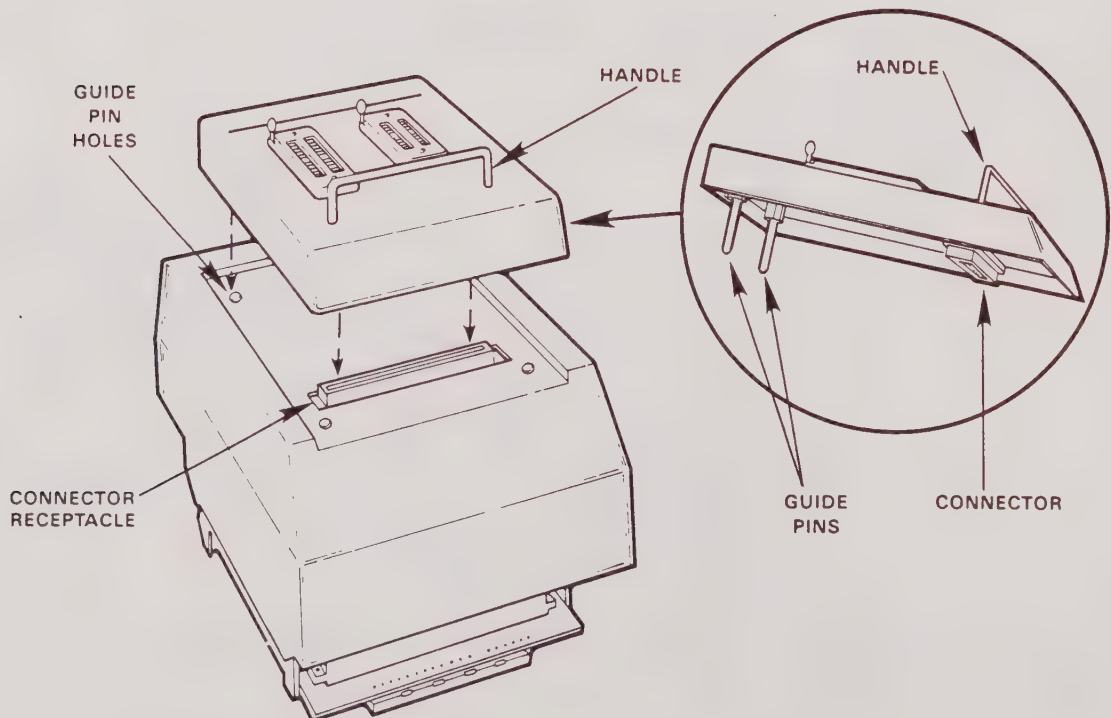


Figure 2-2. Adapter Installation

2.3 REPACKING FOR SHIPMENT

If any equipment is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In any correspondence, identify the unit by name, model number, and owner. Be sure that the shipping container used is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material, and seal well with strong tape. Mark the container DELICATE INSTRUMENT or FRAGILE.

3. CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This section defines the functions of the principal hardware components of the LogicPak and the P/T Adapters. Each major function is depicted by a block diagram accompanied by a written description. The principal components of the LogicPak are illustrated and labeled with their names and part numbers in figure 3-1. Figure 3-2 is a block diagram of the LogicPak electronics. The LogicPak is controlled by the programmer's extended processor bus (J6 in figure 3-2) through the programmer's mating connector.

LogicPak adapters interface with the LogicPak. When these adapters are installed, the LogicPak provides all the specific hardware and firmware required to support numerous families of programmable logic. Support provided includes methods of specifying the logic device design, fuse programming and verification, and functional testing.

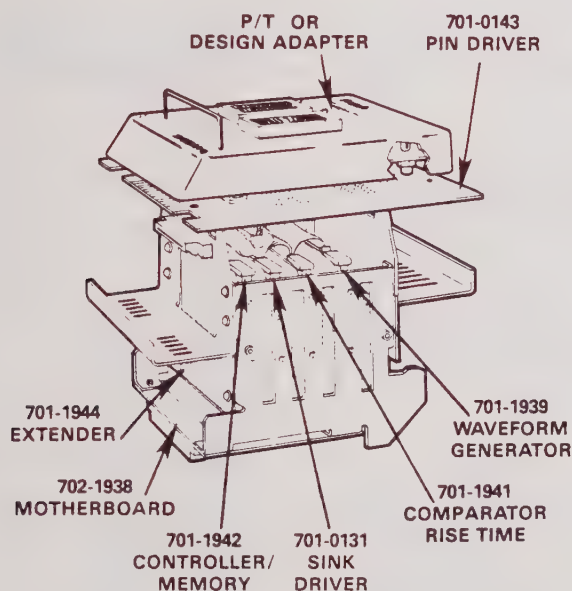


Figure 3-1. Principal Components of the LogicPak

3.2 BLOCK DIAGRAM DESCRIPTION

Each LogicPak board is described, and block diagrams are presented in subsections 3.2.1 through 3.2.7. Schematics are provided at the back of this manual.

3.2.1 Motherboard

The motherboard (702-1938) accepts the programmer processor bus and power supplies and routes them to the five 72-pin connectors. It also serves as the interconnect between the five connectors for signals generated on the plug-in boards.

3.2.2 Bus Extender Board

The bus extender board (701-1944) is installed in one of the five motherboard connectors and extends motherboard pins up to the top-mounted pin driver board (701-0143).

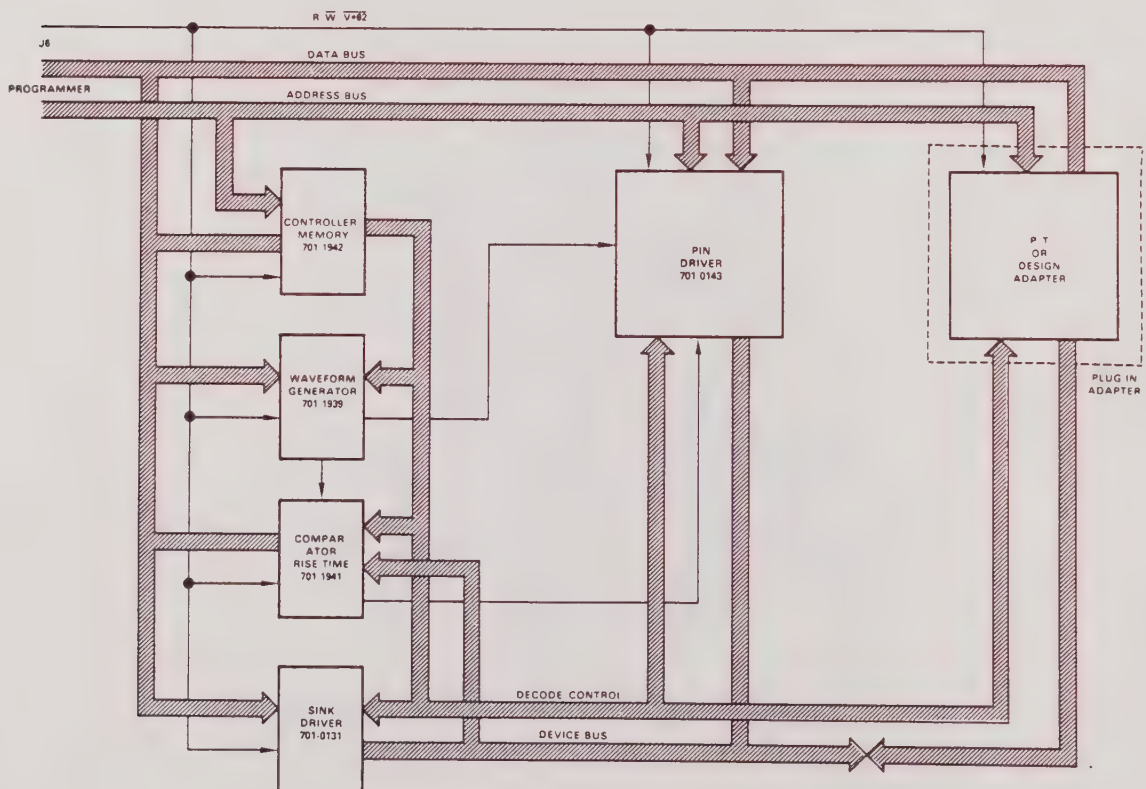


Figure 3-2. LogicPak Block Diagram

3.2.3 Controller/Memory Board

The controller/memory board (701-1942) has two functions: 1) It provides high-speed control operations that are not obtainable under processor operating speed, and 2) it contains the address decode circuitry that specifies the memory map for the base LogicPak and adapters. The block diagram of the controller/memory board is in figure 3-3.

CONTROL FUNCTION

A high-speed controller is necessary to supplement the programmer's processor because of the large quantity of serial data that must be read during programming, verifying, and testing of logic devices; see the controller portion of figure 3-3. A free-running crystal-controlled oscillator produces a 4-MHz clock pulse that synchronizes the on-board operations of the control counter, vector counter, synchronize register, and control register. Its output is routed to other boards via the motherboard. The mode register stores instructions from the processor that are presented to the controller and test PROM; these instructions describe which high-speed cycle the controller should perform.

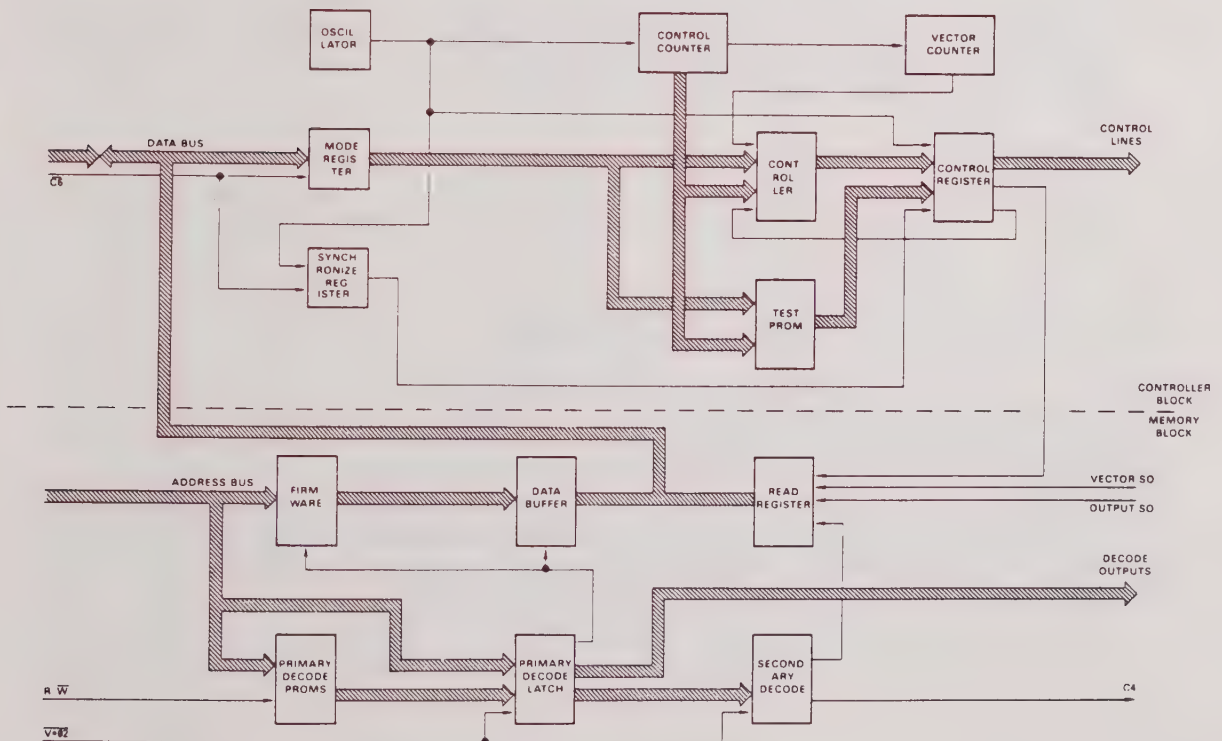


Figure 3-3. Controller/Memory Board Block Diagram

During each cycle, the control counter addresses the controller and the test PROM. Their decoded output function determines what control states should exist for that cycle. These states, which are in the form of registered control lines, are routed to other cards to control the input and output register operations. Each cycle is executed by output from the synchronize register. This output synchronizes the processor operations to the controller cycles. This synchronization is a handshake, busy/ready-type operation.

At the end of each cycle, data serially stored (under controller operation) in the read register are available for interrogation by the processor. These data represent: 1) logic device fuse states after fuse-related operations, 2) device output data during functional test operations, or 3) the Logic Fingerprint test. During the Logic Fingerprint test, a vector counter tallies 128,000 cycles and then outputs a signal that tells the processor that one Logic Fingerprint test cycle has been completed. The test can then end or continue, based on user-selectable options. The test options range from 0 (no test performed) up to 99 cycles.

MEMORY FUNCTION

The two parts of the memory function are: 1) primary decode, and 2) storage of LogicPak firmware; see the memory portion of figure 3-3.

1. Primary decode. The decode PROMs and decode latch allocate the available 16K bytes of processor memory to LogicPak functions. Where necessary, the output from the decode latch is routed to the secondary decode on other boards. Decode outputs are timed with V02 such that the selected locations are strobed to the data bus only during V02 time.
2. LogicPak firmware. The low-order 8K bytes of the 16K byte available space are allocated for LogicPak firmware. This firmware is stored in a 16K-byte PROM organized as two 8K-byte pages, selected by the page register, U16. The outputs of the PROM are buffered and presented to the data bus.

3.2.4 Waveform Generator Board

The waveform generator board (701-1939) selects specific voltage levels required to perform logic device fuse read, fuse program, and functional test operations. Figure 3-4 is a block diagram of the waveform generator board. The three major power supplies of the waveform generator are VCC supply, CE supply, and BIT supply. Each supply is under software control via a DAC (digital-to-analog converter). The DAC voltage output levels are obtained by presenting data via the data latch to the DAC inputs. This latch provides buffering and the timing required to store data. A common DAC reference voltage is generated from the DAC reference voltage circuit.

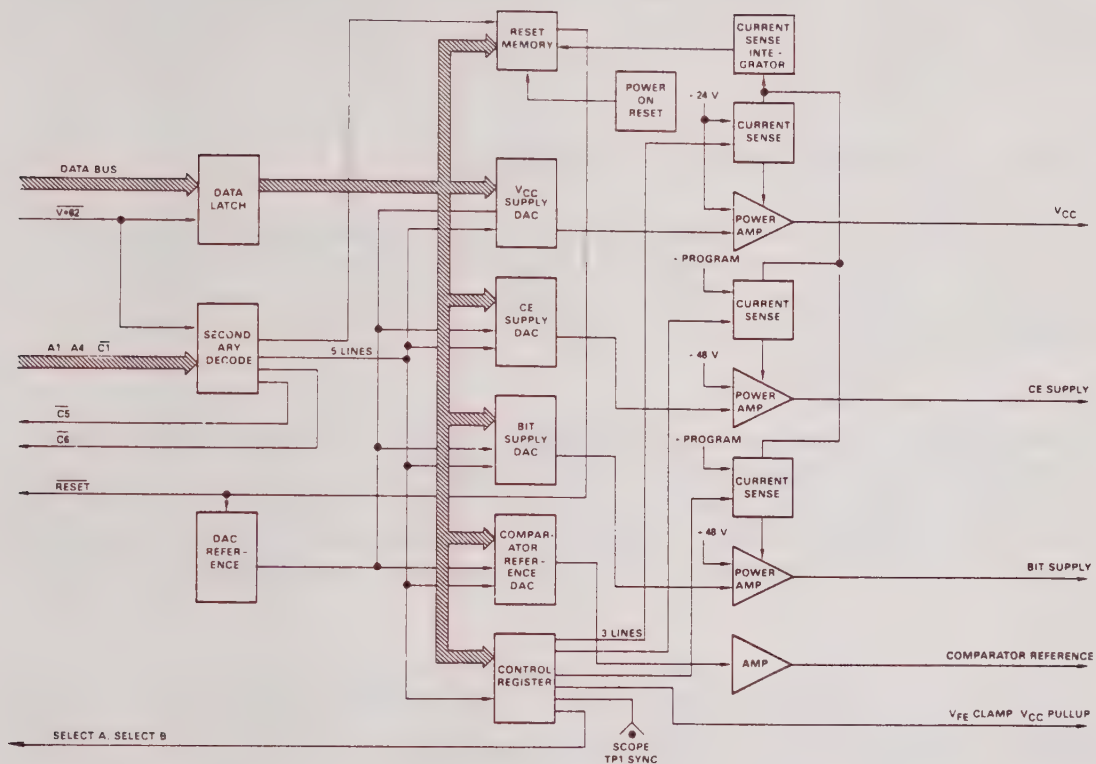


Figure 3-4. Waveform Generator Block Diagram

Each DAC output is routed to a power amp to provide for the high current requirements of the supplies. The power amps are op-amps with their positive voltage rails supplied through current sense detectors. The output rise and fall times are fixed by the slewing rate of the op-amp and are routed to the rise time section of the comparator/rise time board (T/rise comparator).

The current sense detectors have two selectable ranges. The ranges are controlled by the values stored in three bits of the control register. When activated, these detectors set the reset memory, which in turn kills all supply outputs by shutting down the DAC reference. The state of the reset memory is gated onto the data bus, and, if the memory state is set when inspected, an overcurrent error is flagged. The power-on reset circuit sets the reset memory when the programmer is powered up. When a device-related operation is selected, this memory is cleared by an initialize routine and remains cleared until an overcurrent condition sets the memory or the programmer is powered down. The current sense integrator smooths the transient overcurrent pulses, thereby avoiding false overcurrent errors.

Other functions of the control register are scope synchronization and provision of control lines for the adapter. These lines control the adapter LEDs, the backward device test circuitry, and the special clamping levels.

The comparator reference supply is identical in operation to the three other supplies except it does not require (or incorporate) a power amplifier and current sense stage. Its output is routed to the comparator section of the comparator/rise time board and is used as a programmable voltage reference level for the comparators.

3.2.5 Comparator/Rise Time Board

The comparator/rise time board (T/rise comparator) (701-1971) has two functions: 1) It monitors the logic device pins and the waveform generator outputs, and 2) it converts the waveform outputs into switchable signals with programmable rise time control. Figure 3-5 is a block diagram of the comparator/rise time board.

RISE TIME FUNCTION

The switch control register determines which rise times are selected and which switches are to be activated. Each rise time control circuit consists of a current source (one common current value for all sources) driving the base of its switch transistor to charge the base capacitance. When the bases are released, a linear ramp is generated that is truncated at the switch supply level. The slew (dV/dt) rate is dependent on the value of capacitance switched to ground by the control register and the value of the current source.

The switch outputs and the nonswitched VCC sense line are connected to the switch comparator. This comparator allows the switch and VCC functions to be output as status to the status gate. Controller-ready status along with the switch/VCC status are monitored on the data bus. Error codes are displayed if the switches or VCC are not functional during the LogicPak self-test.

COMPARATOR FUNCTION

The comparator monitors the pins of the logic device and compares them against the comparator voltage reference level. The comparators support the high-level program voltages and the TTL read levels of the device. Their outputs (device data) are stored in the output registers that, in turn, output data over the serial output (SO) line to the read register on the controller board. The register load and serial shift operations are synchronized to the controller operations by the control line (S/L) and oscillator (CP). As previously explained in subsection 3.2.3 (control function), this is how the logic device fuse and functional status are read.

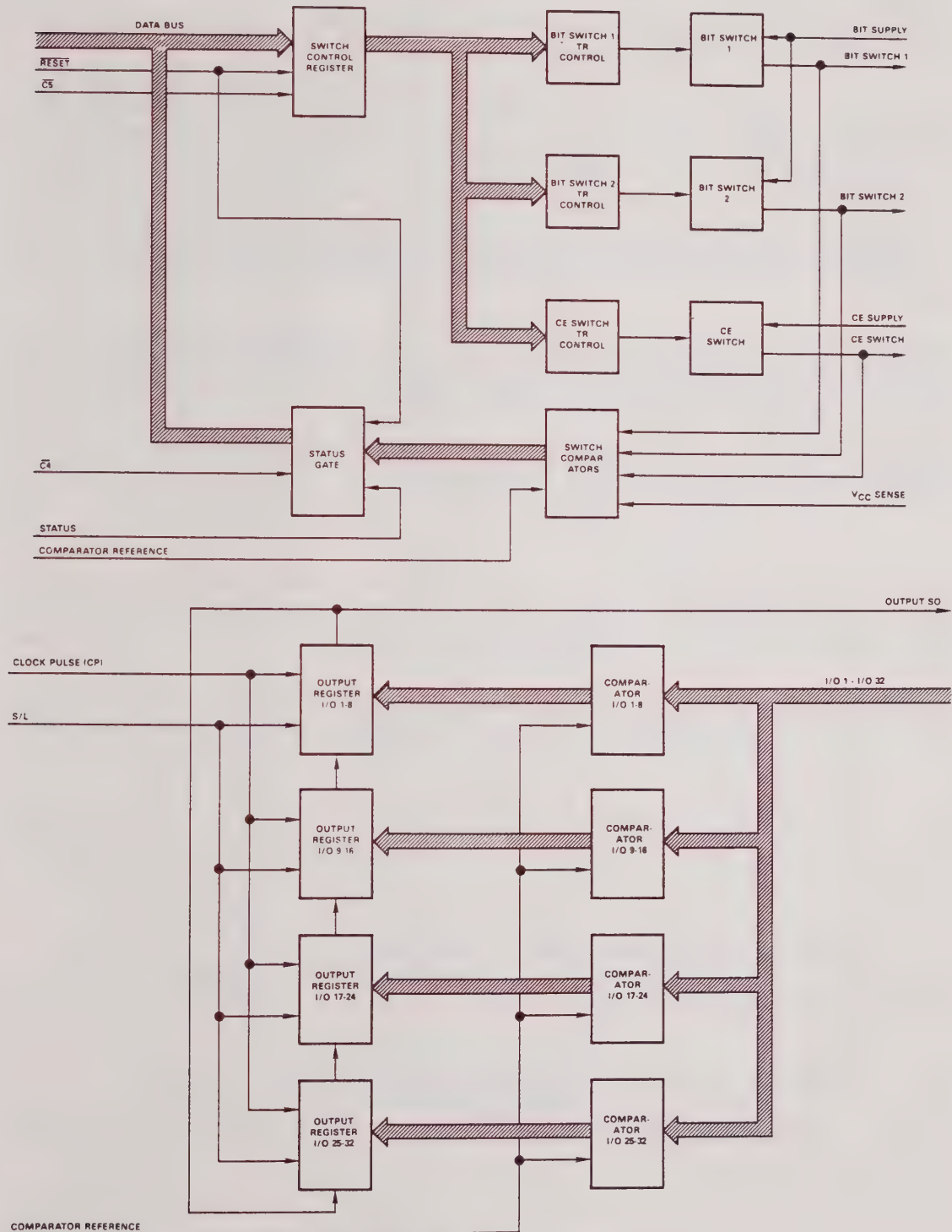


Figure 3-5. Comparator/Rise Time Block Diagram

3.2.6 Pin Driver Board

The pin driver board (701- 0143) serves as a receptacle for the LogicPak socket adapters and contains the source driver circuitry that routes the switch outputs from the comparator rise time board (BIT switch 1, BIT switch 2, CE switch) to the socket adapter receptacle. Figure 3-6 is a block diagram of the pin driver board.

The source drivers are PNP transistor switches driven by current sources that are controlled by the source registers. The current sources provide a constant-base drive to the PNP switches at all switch voltages.

The data latch provides the buffering and the timing required to store data in the CMOS source registers. This data storage will control the routing of the BIT switch and CE switch to the socket adapter receptacle.

The pin driver board also connects the sink driver board outputs and the extended processor bus extender board outputs to the socket adapter receptacle.

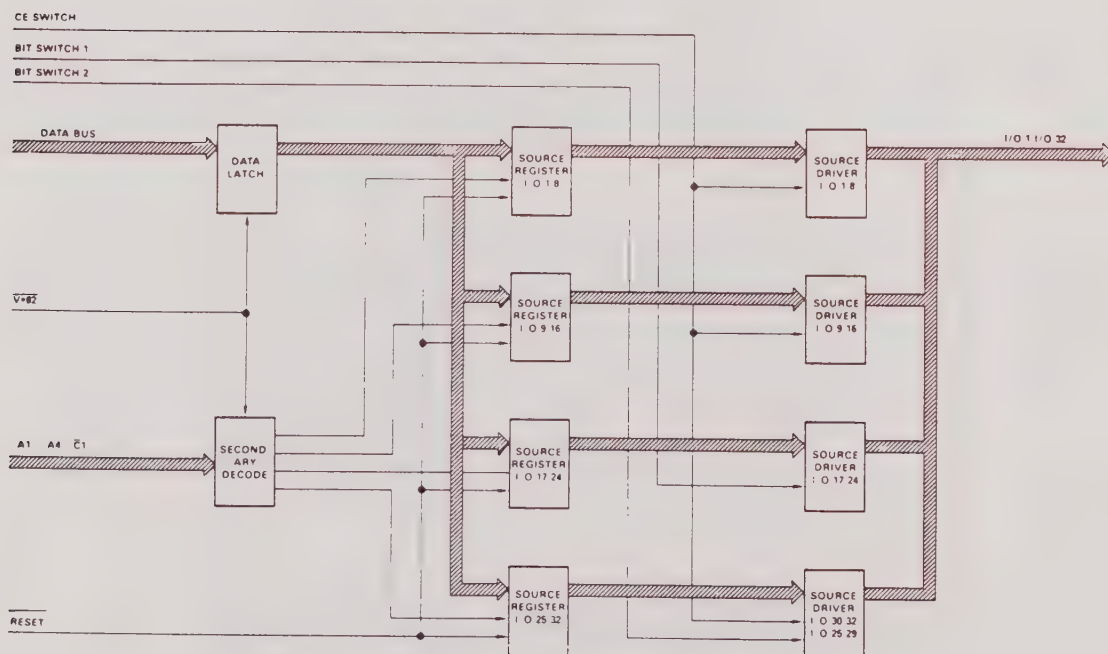


Figure 3-6. Pin Driver Block Diagram

The CP and CE multiplexer changes control of up to four sink drivers from input register control line to controller board control. This alternate control is necessary during the Logic Fingerprint test to provide special consideration to logic devices that have dedicated clock, reset, preset, and enable pins.



3.3 P/T ADAPTERS 303A-001 THROUGH -007, -009 AND -010

A block diagram of the P/T adapter is shown in figure 3-8. The circuitry represented in figure 3-8 for the 303A-001 through -007 adapters is contained on a single printed circuit board while the 303A-009 and -010 adapters consist of two printed circuit boards as shown in figure 3-9. The following description applies to both types of adapters. A schematic diagram for each specific P/T adapter is contained in Appendix B at the back of this manual.

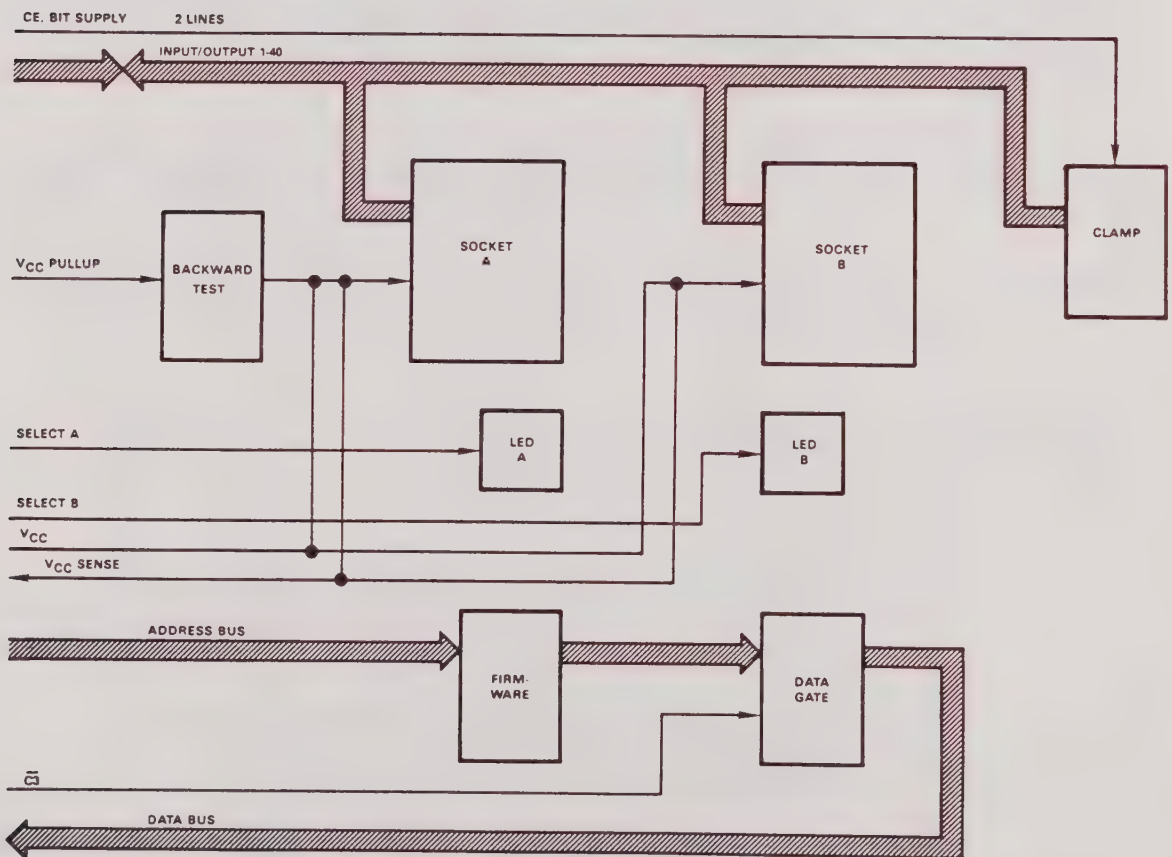


Figure 3-8. Typical P/T Adapter Block Diagram

The P/T adapter routes all signals required to perform fuse operations and functional tests from the LogicPak to the device installed in the socket. When one of the sockets is enabled, the corresponding LED is lighted.

Programming voltage levels are routed to a clamping R-C network which is precharged to the programming voltage potentials. When the programming pulses are presented to the device pins, the network prevents overshoot.

A backward test circuit connects to the VCC pin of each socket. The circuit tests the orientation of the logic device in its socket. If it is incorrect, an error code will be flagged and operation will stop. The test method limits power to the device, thereby preventing damage to it.

Firmware specific to the device manufacturer's family of logic is resident in an EPROM, which receives its address and select inputs from the LogicPak. The EPROM outputs are buffered by a data gate whose outputs feed back to the data base within the LogicPak; fuse programming, verification, and functional testing algorithms are stored in the EPROM and are referenced by stored family and pinout codes.

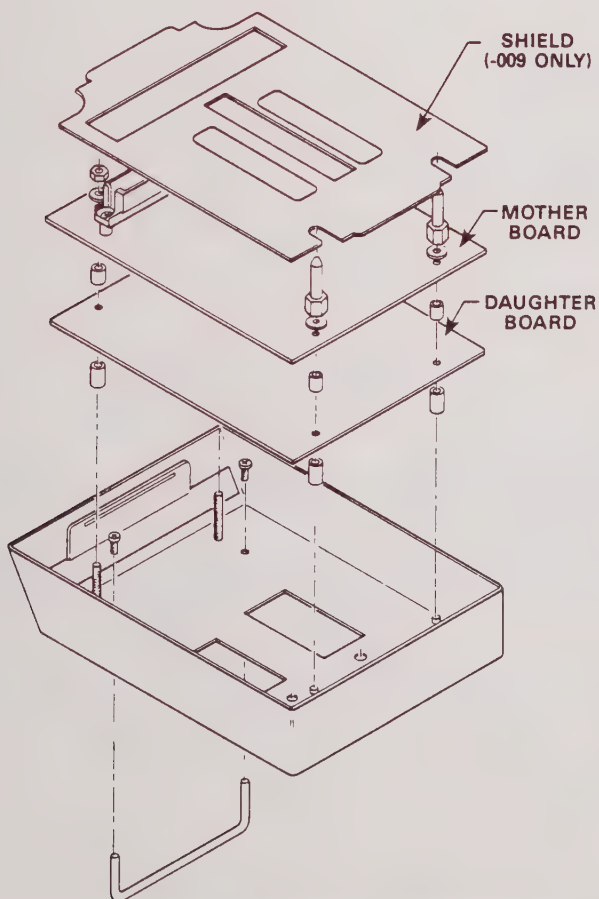


Figure 3-9. 303A-009, -010, -011A/B P/T Adapter Assembly

3.4 P/T ADAPTER 303A-011

3.4.1 General Circuit Description

The 303A-011A DIP and the 303A-011B PLCC P/T Adapters' circuitry are shown in figures 3- 10A and 3-10B. Each P/T adapter consists of a mother board and daughter board as shown in figure 3-9.

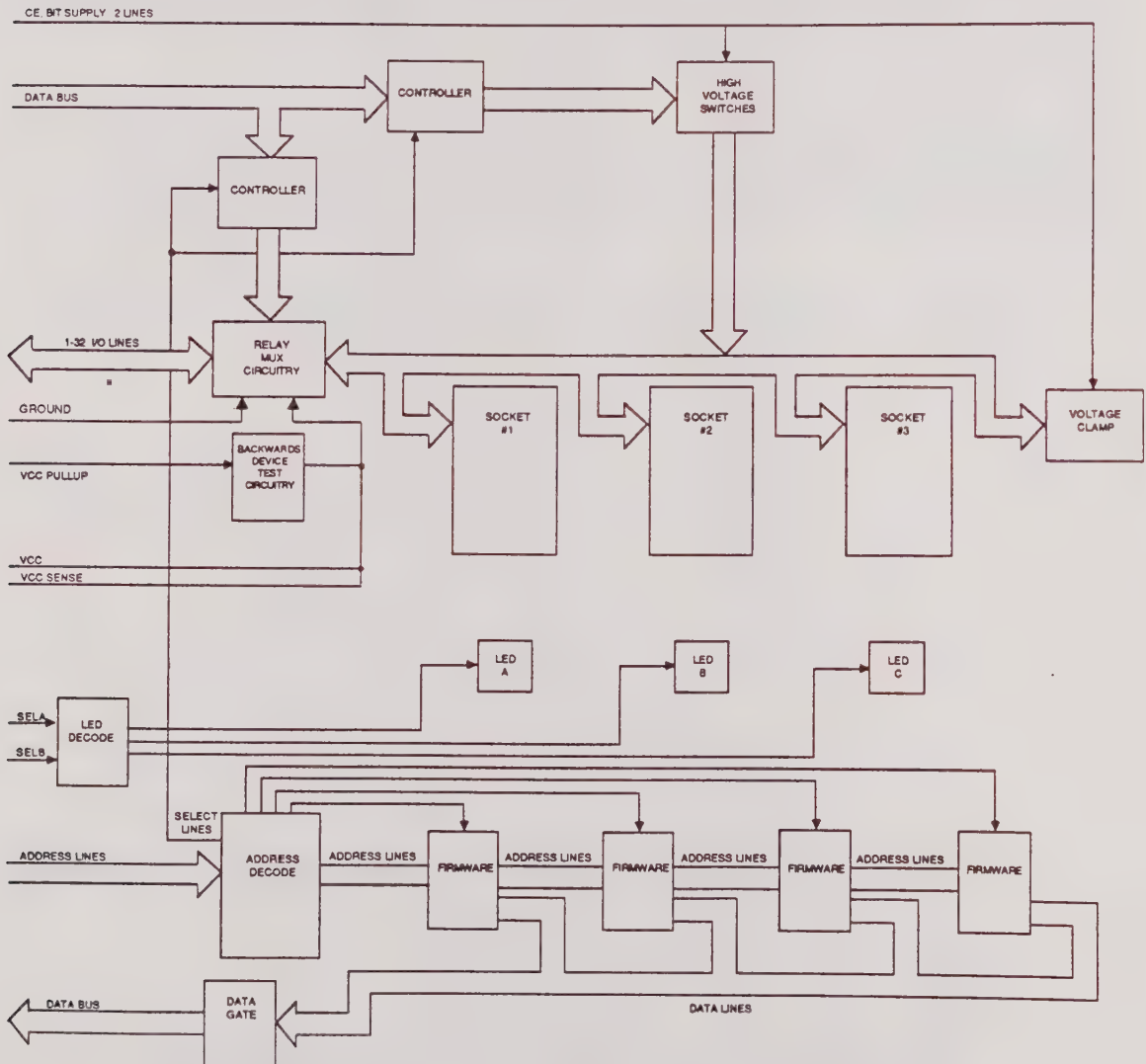


Figure 3-10A. 303A-011A Block Diagram

When the 303A-011A/B P/T adapters are inserted on the LogicPak, the EPROM that contains LogicPak firmware, which resides on the LogicPak controller board, is disabled. The 303A-011A/B P/T adapters contain their own LogicPak firmware, which is located in an EPROM on the P/T adapter motherboard. This EPROM performs the same overhead functions as the one resident in the LogicPak and also has increased capabilities to access new, complex algorithms.

In addition to the basic operating functions described in section 3.3, the 303A-011A/B P/T adapters also contain the following circuitry: high voltage switches, relay multiplexer (MUX) and continuity test. These are described in the following subsections.

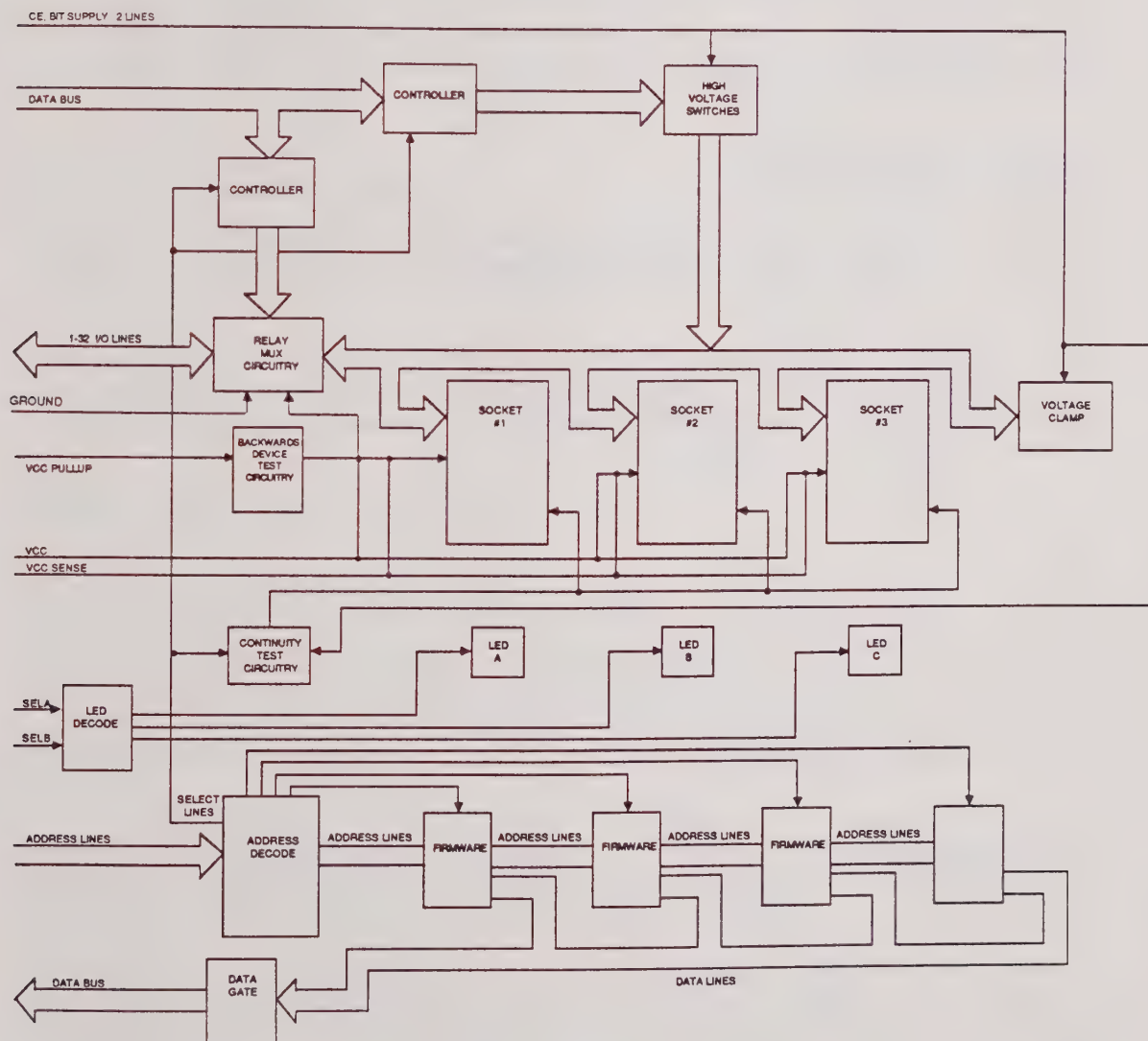


Figure 3-10B. 303A-011B Block Diagram

3.4.2 High Voltage Switches

The high voltage switches enable the BIT supplies to be rerouted to the device pins normally fed by the CE supply. These switches allow for greater programming flexibility since the CE supplied device pins are no longer limited to only one voltage supply.

3.4.3 Relay Multiplexer (MUX)

Through a series of switching relays, a multiplexer (MUX) reroutes I/O lines from the LogicPak to the two 28-pin sockets on the PLCC daughter board. Devices that normally have 24 pins in the DIP package are packaged in the 28-pin PLCC package. The No Connect (NC) pins are different depending on the device pinout type (JEDEC, Altera or MMI) and the MUX routes the I/O lines to the correct device pin depending on the pinout type being used. The relay MUX also is used to route Vcc and GND to different socket pins, in both the DIP and PLCC versions.

3.4.4 Continuity Test

Continuity measurements are made possible by the presence of a substrate diode in the device. See figure 3-11 for a diagram of a typical continuity measurement circuit of a bipolar device: 3-11A shows the 303A-011A's circuitry, and 3-11B shows the 303A-011B's circuitry.

The continuity test begins by first pulling up all device pins through resistors to +5 volts. Each device pin is then individually switched low. A measurement is taken at each pin to verify that the pin is pulled up by the substrate diode. The device pin is then returned high and testing begins on the next pin of the device. The Vcc is tested separately.

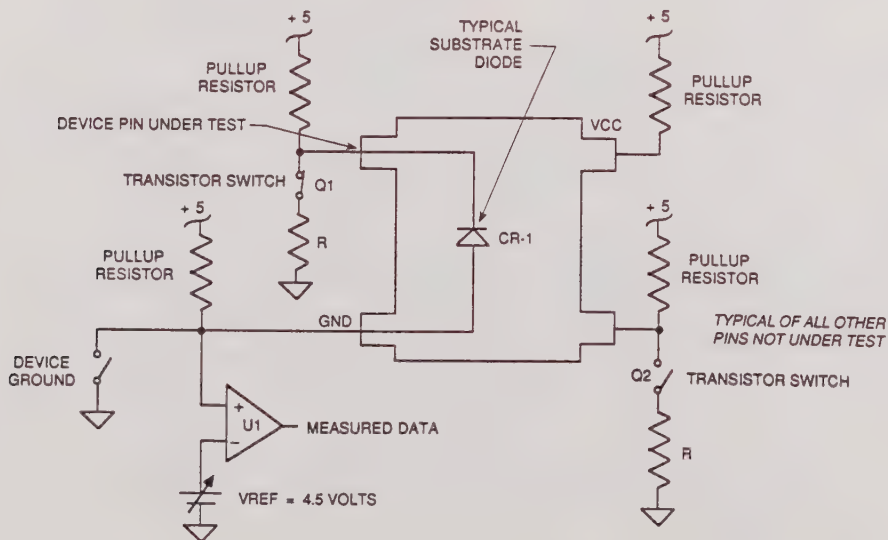


Figure 3-11A. Sample Continuity Test Circuit for 303A-011A Adapter.

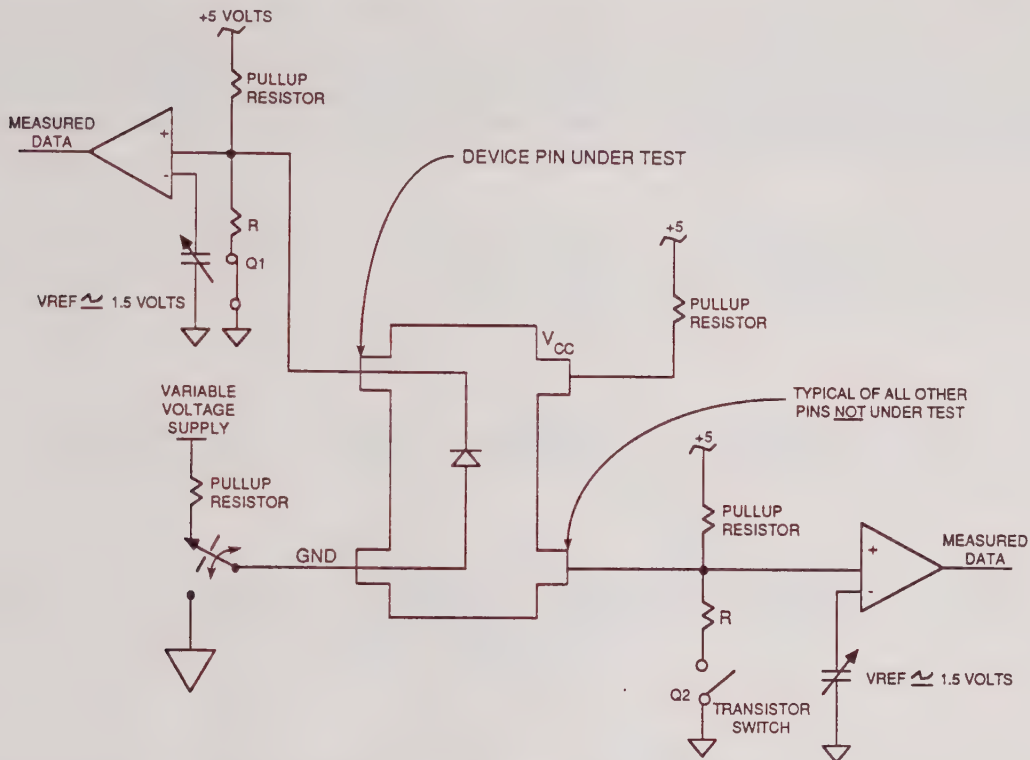


Figure 3-11B. Sample Continuity Test Circuit for 303A-011B Adapter.

3.5 P/T ADAPTER 303A-008

3.5.1 General Circuit Description

The 303A-008 P/T adapter contains all the electronics necessary to interface with the LogicPak on three circuit boards shown in figure 3-12. These three circuit boards, the Memory board, the Intermediate board, and the Socket board contain the electronics to program and test the 32R16 programmable logic device. In addition, all the 32R16 device identity firmware is resident within this adapter.

Figure 3-13 is an overall functional block diagram of the P/T adapter. This diagram illustrates the location of the principal adapter components as well as the signal and bus interconnections between the P/T adapter, LogicPak, and the adapter's circuit boards.

The 303A-008 P/T adapter's circuitry supports twenty-six source drivers. They are functionally equivalent to the 32 source drivers located in the LogicPak. The P/T adapter uses a combination of its own source drivers and some of the LogicPak source drivers (routed via the PLDS I/O bus) to provide all the required voltages and waveforms needed for programming/testing the 32R16 40-pin and 44-pin devices.

Most of the 32R16's active pins require both source and sink drivers. The programming and testing of logic devices requires that these active pins be monitored for voltage level by sense comparators. Therefore, at any given time, at least one of the three types of signals (source, sink or sense) will be present on the device's active pins. As indicated previously, these three signals are supplied by the combined circuitry of both the P/T adapter and the LogicPak.

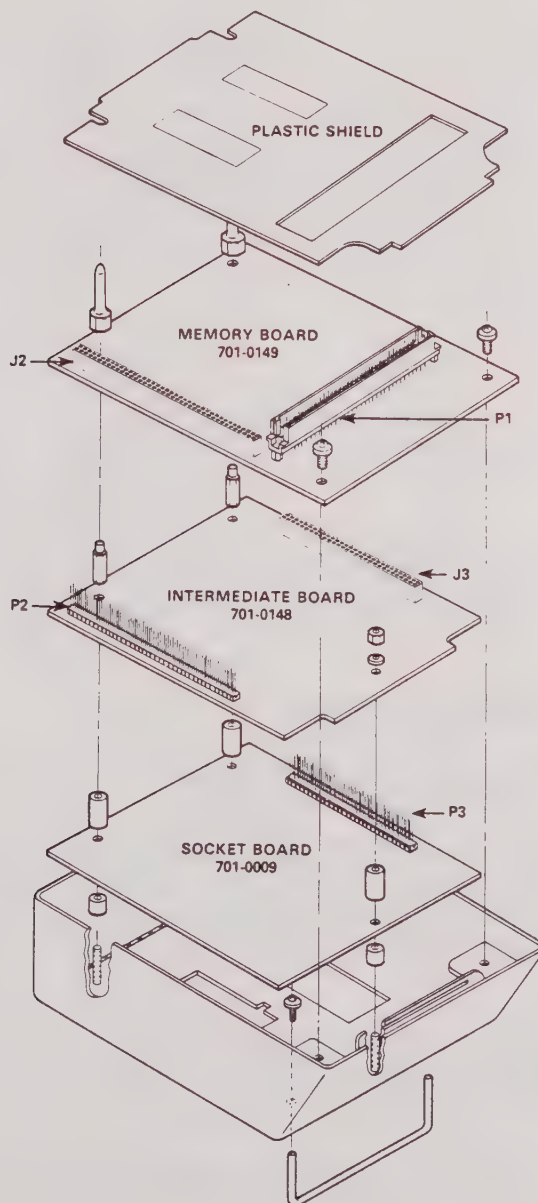


Figure 3-12. 303A-008 P/T Adapter Assembly

Control of the P/T adapter and LogicPak source and sink drivers is provided by the programmer, which receives its instructions from the software resident in the adapter's EPROM. Control signals, address buses, and data buses are routed through various adapter latches, input buffers, sense comparators, decode, and pulse smoothing circuitry.

Supply voltages CE, BIT, and +5 volts are routed through adapter circuit board filters (except Vcc). The BIT supply is used by a DC-DC converter to produce a regulated +20-volt output. The functions of supply filters and the DC-DC converter are described in detail in the description of the Intermediate board. The CE and BIT supplies are current limited to 600 milliamperes.

NOTE

The adapter's pulse smoothing circuitry permits programming pulses to exceed the overcurrent limit, as long as they are limited in duty cycle.

A Device Orientation Tester is designed into the adapter circuitry to prevent destruction of the 32R16 if it is inserted in the device socket(s) incorrectly. For a more detailed description of this circuitry and other adapter board circuits, refer to the detailed circuit descriptions which follow.

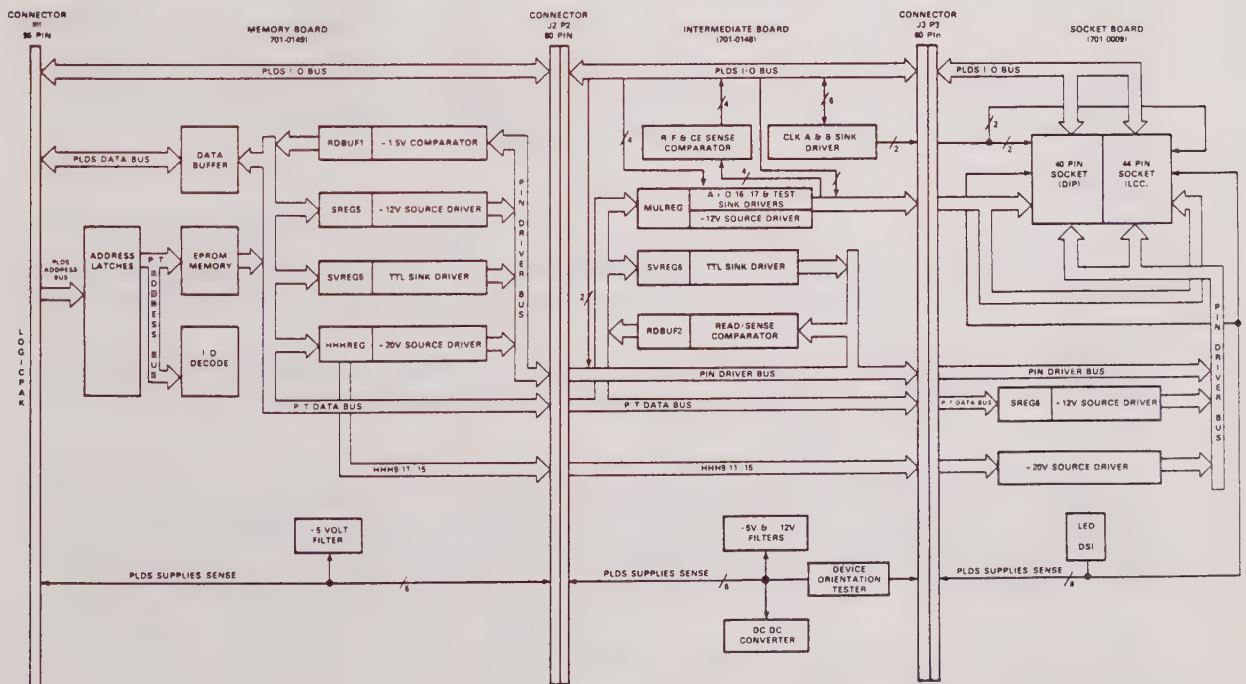


Figure 3-13. 303A-008 P/T Adapter Block Diagram

SOURCE DRIVER CIRCUITS

The source drivers are the same type, whether supplied from +12 or +20 volts. The +20 volt source driver's (U17) operation is described below as an example to explain all the source driver's operation. A Memory board schematic diagram is contained in Appendix B of this manual.

When U17 pin 2 goes to approximately five volts, a constant voltage is set across R7, yielding a constant current through R6. Since C16 is in parallel with R5, the initial current path is through C16 until approximately 0.7 volts is across it, then transistor Q1 turns on. This constant rise in the base-emitter voltage of Q1 yields a fixed rise in the output of the +20 volt source driver of approximately 5 volts per micro-second.

TTL SINK DRIVER CIRCUITS

U2 and U15, in conjunction with their associated resistors, comprise the Memory board's TTL sink driver circuit. This circuit drives the device pins to either the high impedance state or to the low TTL voltage (VIL).

COMPARATOR CIRCUITS

As described in a preceding paragraph, the comparators (U3, U10) monitor the source/sink driver's output voltage to the Pin Driver bus. The output voltage is monitored for each applicable device socket pin and compared to a +1.5 volt reference (VRef). The reference voltage is supplied by the Intermediate board's DC-DC Converter.

All the source and sink driver outputs combine to form the Pin Driver bus. The Pin Driver bus, the P/T adapter data bus, the I/O bus, and a set of I/O Decode (U16) generated control signals are routed to connectors J2-P2 for input to the Intermediate board. The control signals include the source register/sink and register/read buffer signals (CKHHH, CKHH, CKH, RDBFR).

SOURCE, SINK, AND RDBUF REGISTERS

Two source registers and one sink register feed the enable signals, supplied and latched through from the P/T adapter data bus, to +12-volt and +20-volt source and TTL sink drivers. The voltages for these source/sink drivers are supplied by the Intermediate board through the J2-P2 connector interface.

The HHHReg (U11) source register is an eight-bit TTL compatible D-type latch. It feeds the enable signals to eight individual +20-volt source drivers; four (U17) on the Memory board (AI/O 1-3, 7) and four (Q11) on the Socket board (AI/O 9-11, 15).

SReg5 (U12) and SVReg5 (U14) are the same type of device as the HHHReg. The SReg5 source register feeds the enable signals to eight (U18, U19) individual +12-volt source drivers (AI/O 0-7), which are located on the Memory board. SVReg5 (U14) sink register is used to feed eight enable signals to the TTL sink drivers (AI/O 0-7, also located on the Memory board).

RDBuf1 (U13) gates the output of eight sense comparators (U3, U10), when registered, onto the bi-directional P/T adapter data bus. The output of these drivers is compared against a +1.5-volt reference (VRef) to monitor the source/sink driver voltage levels on the Pin Driver bus.

DATA BUS AND BUFFER

The P/T adapter data bus is interfaced to the LogicPak data bus through a bi-directional data buffer (U8). The buffer's data direction is controlled by the R/W signal from the LogicPak. The chip enable for this device is the product of a logical AND function between the V02 and C3 control signal inputs to the decode PAL (U6). (The C3 control signal is active for valid hex addresses 6000 through 9FEF.)

The product of this AND function is the output on pin 12, Ob of U6 (see below):

Oa (pin 19) = Low for: Addresses 9FF8-9FFF

Ob (pin 12) = Low for: Pin 1 Pin 18 + Pin 1 Pin 17

The P/T data bus connects to six source registers (SReg5, 6, SVReg5, 6, HHHReg, MULReg) and two comparator read buffers (RDBuf1, RDBuf2) in the P/T adapter. There are three source registers (as mentioned previously) on the Memory board, two on the Intermediate board, and one on the Socket board. Each source register feeds either +12-volt or +20-volt source drivers, or TTL sink drivers.

3.5.2 Block Diagram Description, Memory Board

The Memory board interfaces to the LogicPak via connector, P1, as shown in figure 3-14. All I/O, data, and address buses, plus control signals, are routed through this connector.

ADDRESS LATCH CIRCUITS

The programmer address bus is latched onto the P/T Address bus through the Memory board Address Latches (U5, U7). Latching occurs during the active state of the V02 signal and is allowed to change when V02 is high (inactive). Latched addresses are routed to both the program EPROM (U4) and the I/O Decode circuit (U6, U16).

I/O (ADDRESS) DECODE AND EPROM

The 32k-byte program EPROM (U4) contains the operating program for the programmer and LogicPak. The I/O Decode circuitry consists of a PAL (U6) and an address Demultiplexer (U16). The PAL is programmed such that its output (pin 19) is active (low) for all hex addresses in the range from 9FF8 to 9FFF. It enables the address Demultiplexer to decode one of the eight addresses within this range from the three lowest order bits of the P/T Address bus.

Four of these decoded addresses (9FF8, 9FFC, 9FFA, and 9FFE; at U16 pins 15, 14, 13, and 12, respectively) are used as chip selects to enable three eight-bit registers (U11, U12, and U14) and one eight-bit buffer (U13). The other four decoded addresses (9FF9, 9FFB, 9FFD, and 9FFF) are routed via connector J2 to the Intermediate board, where 9FF9, 9FFB, and 9FFF are used as chip selects to enable two eight-bit registers (U1, U7) and one eight-bit buffer (U6). 9FFD is routed to the Socket board as a chip select for one eight-bit register (U2).

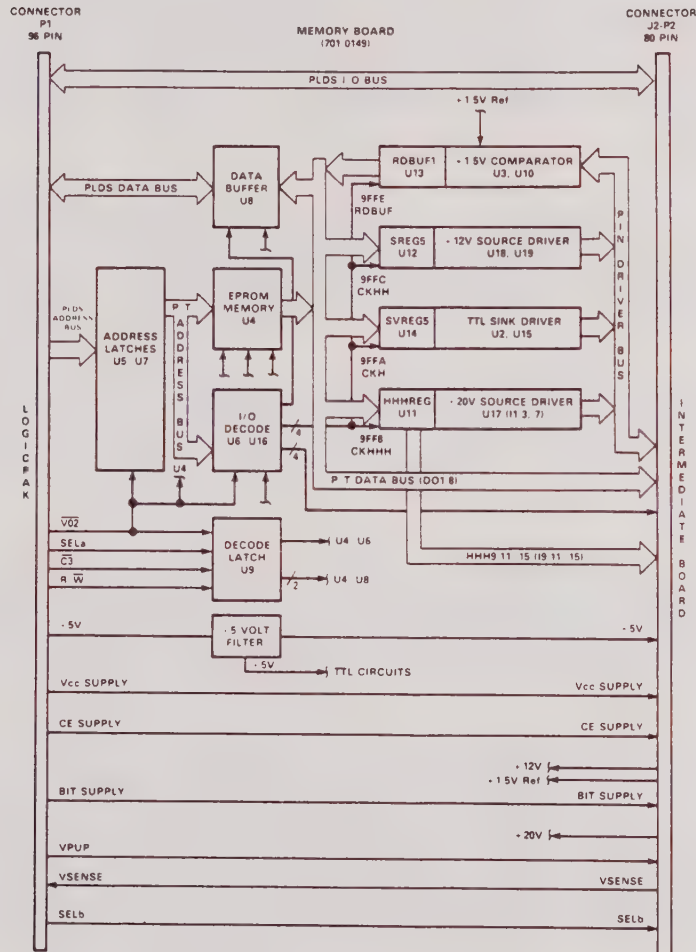


Figure 3-14. 303A-008 Memory Board Block Diagram

3.5.3 Block Diagram Description, Intermediate Board

The Intermediate board performs some functions which are similar to the Memory board, as shown in figure 3-15. However, it also filters and converts the programmer supply voltages and routes these voltages to its own circuits, as well as the other two P/T adapter circuit boards.

P/T ADAPTER SUPPLY VOLTAGES

The +5-volt supply is filtered on the Intermediate board prior to being routed to any circuitry. Test points are provided on both boards to check the +5-volt supply.

The CE supply is filtered by an L-C network (L6, C11) which provides a stable +12 volts. This filtered supply delivers to the source drivers more pulsed current than the CE supply is capable of supplying.

The +12 to +20-volt DC-DC converter provides expanded voltage supply capabilities. It allows the BIT and CE supplies to be set at +12 volts and permits a regulated +20 volts to be available for use where needed.

The BIT supply is protected by a low pass power filter (L1, C17) which shields it from the high, pulsed (switching) current of the +20-volt supply. Without this input filter, the +20-volt supply input current would cause an over-current condition in the BIT supply. The following paragraphs describe the DC-DC converter's operation in component level detail. To follow this description, refer to the Intermediate board schematic diagram in Appendix B.

DC-DC CONVERTER CIRCUITS

The DC-DC converter's +20-volt supply is regulated by the pulse width modulator (U11), the high current choke (L2), the catch diode (CR12), and the pass transistor (Q4). When +12 volts is present at the input of L2, and Q4 is on (low impedance to ground), the current increases through the inductor building up a magnetic field. When Q4 turns off, the current flow is interrupted and the resulting positive voltage at the anode of CR12 (results from the collapse of the magnetic field) raises the converter's output voltage to a higher level than the input voltage. After many initial cycles of this switching action, the voltage on the output capacitor C14 rises to a voltage level (+20 volts) at which point regulation begins.

Regulation is performed by varying the time that Q4 is ON. This varies the magnetic field built up on L2, and in turn, the voltage at the CR12 anode. The output voltage is monitored by the error amplifier inside the pulse-width modulator (PWM, or U11) through the resistor divider network R22, 23, and 25.

L3, L4, and L5, as well as C15 are output filters. The +2.5-volt reference (U12) is used as input to PWM (U11) error amplifier and divided down to +1.5 volts (VRef) as input to the Memory and Intermediate boards' comparators.

NOTE

Pin 19 of U7 is used to enable and disable the DC-DC converter; a logic low enables it and a logic high disables it. This feature is used only in the test mode of the P/T adapter. Disabling the DC-DC converter forces the output voltage to equal the input voltage (minus a 0.7-volt drop).

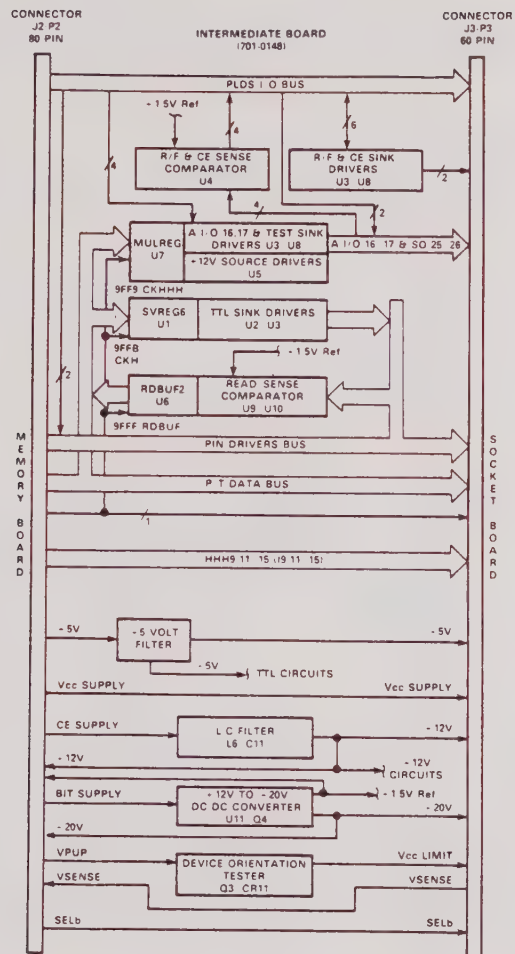


Figure 3-15. 303A-008 Intermediate Board Block Diagram

SOURCE, SINK, AND RDBUF REGISTERS

As previously stated, many Intermediate board functions are similar to the Memory board. The reason for this is that the Intermediate board has many of the same components as the Memory board and they are used for the same purpose. For instance, MULReg (U7) and SVReg6 (U1) are both eight-bit D-type latches and enable the source and sink drivers located on this board.

CE AND R/F SOURCE/SINK DRIVER CIRCUITS

MULReg (U7) performs a number of functions. Pins 2 and 5 of U7 enable the +12- volt source drivers (U5). These source drivers connect to the CEa, CEb, R/Fa and R/Fb pins of the 32R16 installed in the socket. Pins 6, 9, 12, and 15 of U7 enable the drivers (U3, U8) to sink current from the 32R16 CE and R/F pins through a 2K ohm resistor to ground. The sink drivers (U3, U8) also require four other signals that enable the CE and R/F pins to be pulled through the 560 ohm resistors to ground. These additional four signals are provided over the LogicPak I/O bus (I/O 1-4). The I/O bus also supplies the two signals (SO 25, 26), which provide the source drive for the 32R16 CE (CEa, CEb) pins.

SVReg6 (U1) enables another set of TTL sink drivers (U2, U3) on the Intermediate board. The sink driver outputs expand the Pin Driver bus, which is monitored and compared to a +1.5-volt reference (VRef) by the Read/Sense comparators (U9, U10).

READ/SENSE COMPARATOR CIRCUITS

The result of the Read/Sense comparators (U9, U10) is gated onto the P/T adapter data bus, by RDBuf2 (U6), which is an eight-bit buffer.

CLK A AND B SINK DRIVER CIRCUITS

U3 circuits (mentioned previously) that are not used in the CE and R/F application, function as CLK A&B sink drivers. These two circuits are directly enabled by the PLDS I/O bus signals SI 25 and 26. In conjunction with the PLDS SO 29 and 32 source drive signals, and the SI 30 and 31 sense signals, the CLK A&B sink drivers provide the fast rise-time clock signals to the 32R16. In these two clock driver circuits, the 220 ohm pull-ups (R2 and R17) are the low impedance path to +5 volts for the fast risetime. The 220 ohm series resistors (R3, R16) provide protection for the 7407s. The 1N4148 diodes (CR9, 10) block current flow from the clock sink drivers onto the I/O bus.

DEVICE ORIENTATION TESTER

The device orientation tester (Q3, CR11) supplies a limited current to the Vcc pin on the device sockets to protect the 32R16 while determining its orientation in the socket. The sense signal (VSEN), which carries the device orientation information, is connected (along with a Vcc current limit output from the tester) to the Vcc supply line that connects to both device sockets.

The source (R/F pins), sink (R/F and CE), and CLK A&B drivers outputs are loaded onto the pin driver bus. The pin driver bus, the P/T adapter data bus, and the I/O bus are tied to connectors J3-P3 for input to the Socket board.

3.5.4 Block Diagram Description, Socket Board

The Socket board contains the two device sockets (XU1, XU3). XU1 is the 40-pin DIP socket and XU3 is the 44-pin socket (either ceramic leadless or plastic leaded, depending on the P/T adapter configuration). This circuit board also contains two sets of source drivers (+12 and +20 volts), one source register (SReg6), and an LED indicator (DS1); see figure 3-16. DS1 is an LED which indicates the readiness of the adapter to accept devices for programming and testing.

SOURCE REGISTER CIRCUITS

The SReg6 source register is an eight-bit TTL compatible D-type latch. This latch feeds the enable signals, latched through from the P/T adapter data bus, to eight (Q1, Q8) individual +12-volt source drivers which are located on the socket board. This source register is located at address 9FFD and is enabled by the CKHH signal from the I/O Decode circuit on the Memory board.

SOURCE DRIVER CIRCUITS

Four +20-volt source (pin) drivers located on the Socket board receive their enable signals (HHH9-11, 15) from the HHHReg source register, located on the Memory board. The outputs of both the +12 and +20-volt source drivers become part of the Pin Driver bus, and along with the I/O bus, are routed to both the 40-pin and 44-pin device sockets.

The Intermediate board CLK A and B sink drivers and the R/F and CE source/sink drivers outputs are also routed to the device sockets. All the necessary voltages and control signals required to program/test the 32R16 are provided by the Vcc supply, the CLK A and B, R/F and CE circuit outputs, and the I/O and Pin Driver buses. These voltages and control signals are produced by combining LogicPak capabilities with the 303A-008 P/T adapter features.

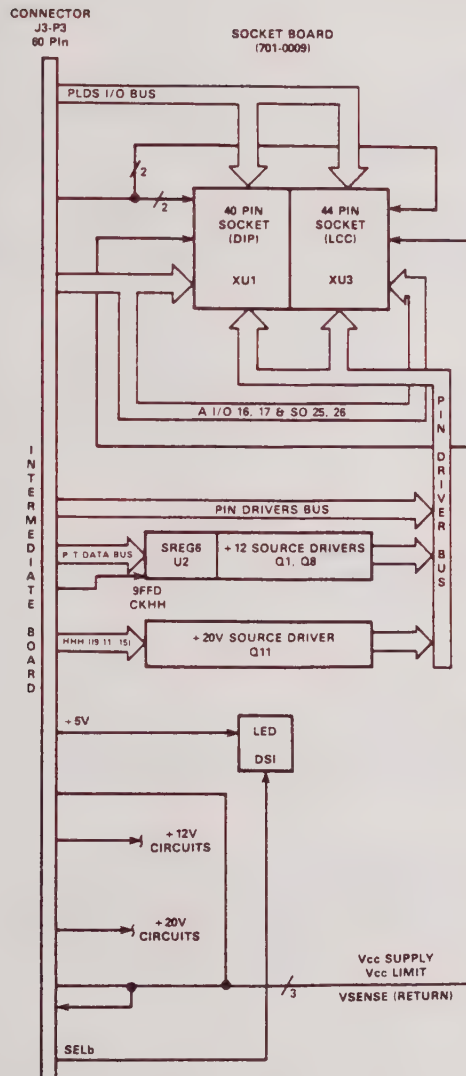


Figure 3-16. 303A-008 Socket Board, Block Diagram

3.6 P/T ADAPTER 303A-012

3.6.1 General Circuit Description

The 303A-012 AIM P/T Adapters' circuitry is shown in figure 3-17. The adapter's circuitry is contained on a Mother board (701-2105) and Socket board (701-2104), which are joined via connector J1.

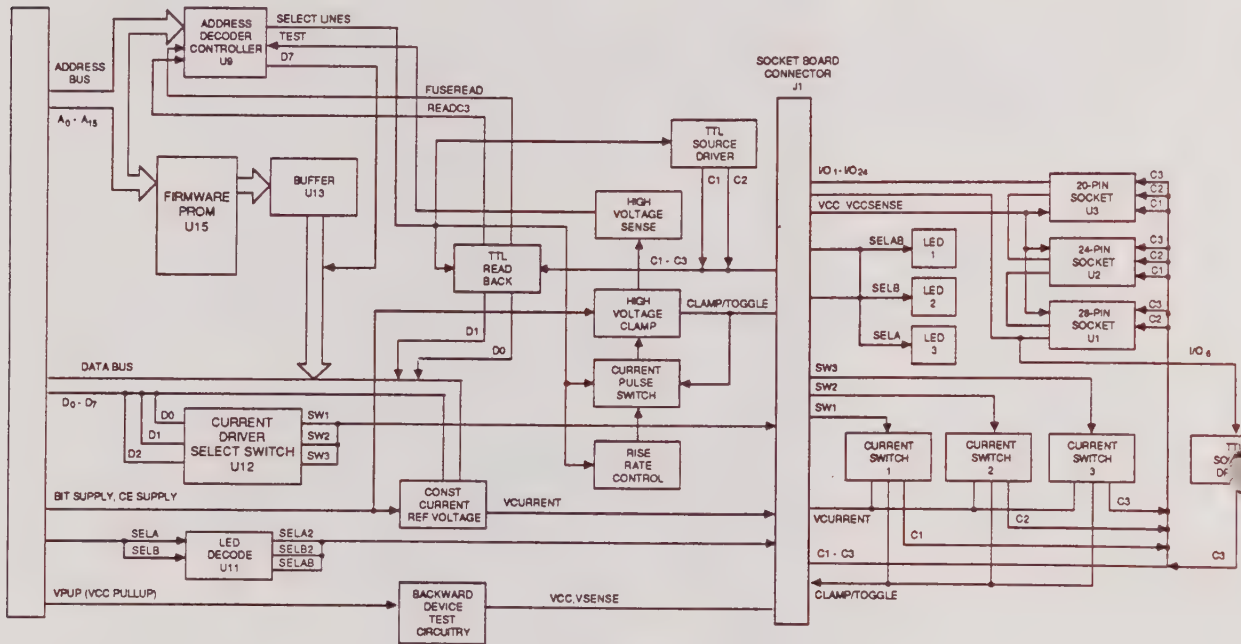


Figure 3-17. 303A-012 Block Diagram

3.6.2 Motherboard

INTRODUCTION

The AIM P/T Adapter's Motherboard is connected to the LogicPak via connector J2. When the P/T adapter is inserted on the LogicPak, the LogicPak's EPROM is disabled. The P/T adapter contains its own LogicPak firmware, located in PROM U15 on the P/T adapter Motherboard.

DECODING

Address decoding is performed by controller U9. U9 is enabled whenever a low is output from the positive-NAND gate, U14. U9 outputs Select signals for TTL readback, Rise Rate Control, Current Switch, Current Driver Select and High Voltage Sense circuits on the Motherboard.

Illumination of the P/T adapter's three LED's is accomplished by a 3-to-8 decoder, U11. SELA and SELB, LED select signals from J2, are fed into U11. U11 then outputs via SELA2, SELB2 or SELAB, which are routed to J1.

VOLTAGE SUPPLIES

The LogicPak's BIT SUPPLY and CE SUPPLY lines feed into Constant Current Reference Voltage circuitry on the Motherboard. D0-D7 are input to A-to-D converter U5. Output voltage from U5 is then routed to the Socket board via the VCURRENT line.

HIGH VOLTAGE CLAMP

High voltage clamp circuitry is used to hold the current pulse to a predefined voltage level, set by the variable A-to-D converter, U5. The clamp circuitry contains a high voltage sense comparator which senses the high voltage flowing through the clamp circuit.

SOURCE DRIVER CIRCUITS

A low on 4BITWR from controller U9 enables the Current Driver Select Switch, U12. D0-D2 are fed into U12, which outputs current switching information on SW1- SW3. SW1-SW3 then enable current switch circuitry on the Socket board.

TTL source circuitry, enabled by a low on 8BITWR, consists of latch U7, CR8 and CR10. Output are signals C1 and C2. C1-C2 are then read back to TTL Readback circuitry, enabled by the 8BITRD line from U9. The Readback circuitry consists of U2, U3 and part of U8. Information is then output via D0 and D1 on the data bus, and via READC3 and FUSEREAD to controller U9. C3 is read back through controller U9.

CURRENT PULSE SWITCH

Current Pulse Switch circuitry is contained in Q7 and Q4. Signals from controller U9 toggle the current source on and off via Q7. Q4 enables switching in a fast or slow rise rate.

PROTECTION CIRCUITRY

Backward Device Test circuitry on the Motherboard consists of Q5, CR12 and various resistors. The sense signal (VSENSE) carries the device orientation information. VSENSE is connected to the Vcc supply line, which is connected to all the device sockets.

3.6.3 Socket Board

The 303A-012 P/T adapter's Socket board houses the high voltage source driver, the current switches, device sockets and device LEDs. Programming information is fed from the LogicPak and Motherboard via I/O lines 1-24.

Current switch circuitry consists of U4, parts of Q1-Q5 and various RC components. Current switch 1 is enabled by SW1, switch 2 by SW2, and switch 3 by SW3.

TTL voltage for C3 is switched via I/O line I6. The switching circuitry consists of parts of Q5 and Q6. This circuitry provides a low impedance input to the socketed device.

Three LEDs on the Socket board indicate which one of the three sockets is active during device operations.

4. MAINTENANCE

4.1 OVERVIEW

WARNING

The instructions in this section are for qualified service personnel only. Do not attempt to perform them unless you are qualified.

The support material in sections 4, 5, and 6 has been provided to help you keep your LogicPak in good operating condition. General maintenance practices are discussed in section 4, calibration procedures are presented in section 5, and basic troubleshooting is described in section 6. General maintenance of the LogicPak consists of cleaning (subsection 4.2) and inspection (subsection 4.3).

4.2 CLEANING

Inspect the LogicPak inside and out for accumulated dirt or dust. To clean the LogicPak, proceed as follows:

1. Wipe any dust or dirt off the outside of the LogicPak with a clean, damp cloth.

NOTE

Do not use abrasive cleaners or solvents that will etch the paint.

2. Remove dust from the circuit boards with a blast of dry compressed air or a clean soft-bristled brush.

4.3 INSPECTION

You can help prevent malfunctions by periodically inspecting your LogicPak. Check cable connections, card seating, component mounting, etc., for shorts, opens, or discontinuities.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating to prevent further damage.

5. CALIBRATION

5.1 GENERAL

WARNING

The instructions in this section are for qualified service personnel only. Do not attempt to perform them unless you are qualified.

This section, in conjunction with the calibration procedure contained in appendix A, contains the information necessary to perform periodic and post-repair calibration of your LogicPak. The need for calibration varies with the amount of use your LogicPak receives. Generally, we suggest calibration whenever:

- programming yields fall below the manufacturer's recommended minimums
- when troubleshooting and repair have been completed
- if the user's company policy requires periodic calibration certification.

5.2 MEASUREMENT CHARTS

Because the LogicPak must be calibrated with a P/T adapter installed, and because calibration values vary with different adapters, you must be sure to use the measurement chart specific to the P/T adapter installed in the LogicPak at the time of calibration. For example, to calibrate the LogicPak with the 303A-011A P/T adapter installed, refer to the Calibration Procedure table located behind the 303A-011A P/T ADAPTER tab in Appendix A.

Each procedure (table) presents the calibration information in columns having the following headings:

- Test Name — indicates the nature of the calibration test being performed.
- Test Connections — tells at which socket pins or circuit board test points to measure voltages.
- Measurement Limits — specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the LogicPak until the problem is corrected.
- Adjustment Location — tells which potentiometer to adjust for calibration.
- Comments — gives special instructions to complete the step.

5.3 CALIBRATION SETUP

The following equipment is required to calibrate the LogicPak:

- 3-1/2 digit digital multimeter (Fluke 8050 or equivalent)
- Dual-trace oscilloscope (Textronix 465 or equivalent)

NOTE

If you do not have the equipment necessary to perform calibration and repairing procedures, contact the nearest Data I/O Service Center. Because of the different programmer mainframes and adapter modules, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak.

To prepare the LogicPak for calibration, proceed as follows:

1. Remove the adapter (if any) from the LogicPak.
2. Remove the four Phillips-head screws from the LogicPak cover (see figure 5-1).
3. Remove the two Allen screws on each side of the LogicPak cover (see figure 5-1).
4. Lift the cover off the circuit board cage assembly.
5. Plug the adapter into the connector on the pin driver board, as shown in figure 5-2.

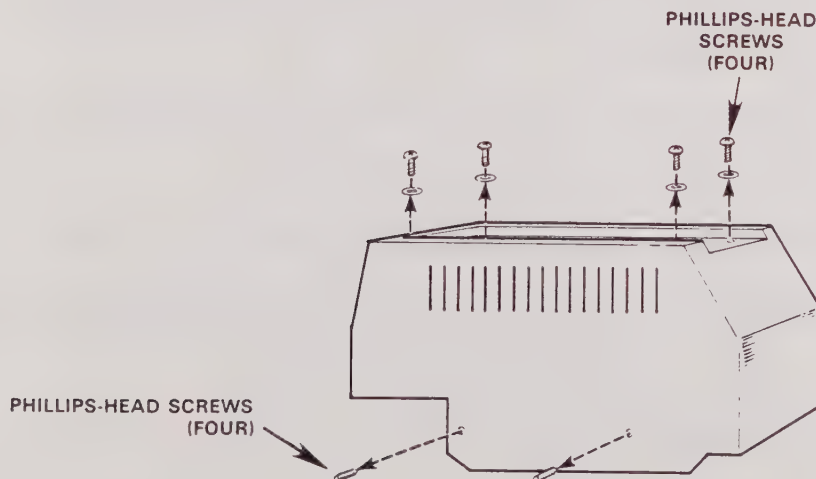


Figure 5-1. LogicPak Cover Removal

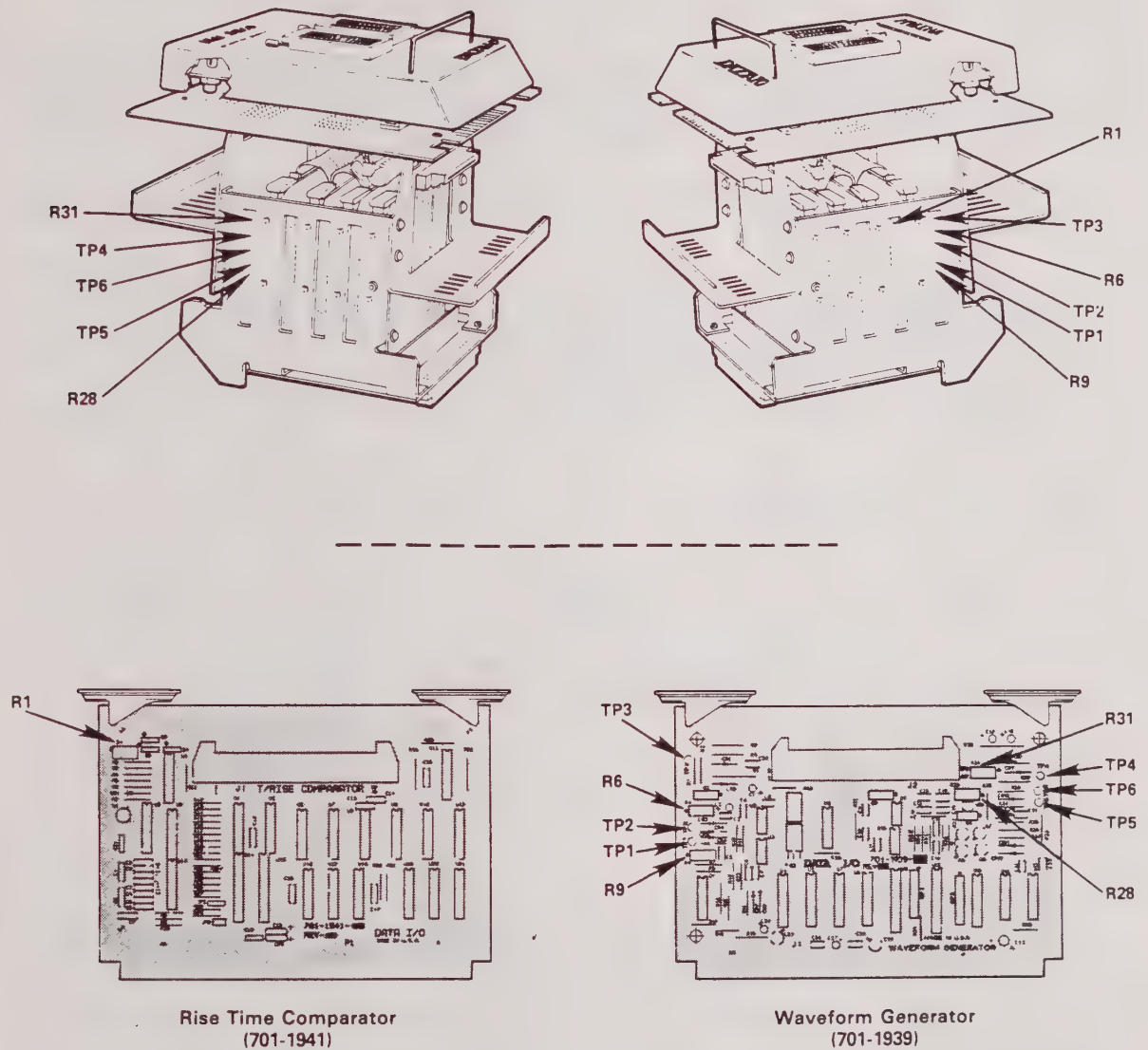


Figure 5-2. Test Point and Adjustment Locations

5.4 CALIBRATION PROCEDURES

5.4.1 Introduction

Calibration of the LogicPak and adapter consists of two distinct procedures:

1. Power supply calibration — measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to the programmer manual for power supply calibration details.
2. DC calibration — consists of measuring and adjusting critical DC voltage levels generated by the LogicPak and by the adapter.

As outlined above, the first step in calibrating the LogicPak is to measure the programmer power supplies (and adjust if necessary). Proper LogicPak operation requires calibrated programmer power supplies. These measurements are essential before any tests are performed on the LogicPak itself. Because power supply calibration varies with the type of programmer you are using, refer to the specific programmer manual for power supply calibration details. DC calibration is described below.

5.4.2 DC Calibration

CAUTION

Remove all devices from the sockets before entering the calibration mode. Calibration voltages may damage any device left in the LogicPak socket.

Proceed with DC calibration as follows:

1. Turn the programmer power on.

NOTE

If left in any of calibration steps 1 through 7 for longer than five minutes without a front panel key depression, the machine will reset itself.

2. Put the programmer in the calibration mode by following the key sequences in table 5-1. The table also explains how to increment or decrement the step number and how to enter calibration at an advanced step (required during waveform observation).
3. Perform the steps contained in the appropriate (that matches the installed P/T adapter) calibration procedure located in Appendix A.

CAUTION

If the LogicPak fails the second step in the calibration procedure, **DO NOT** proceed to the next step. The hardware must pass this step, or further calibration attempts may damage the LogicPak.

If the LogicPak fails any step in the calibration procedure (Appendix A), do not continue to the next step. If error codes are displayed, refer to table 5-2 or 5-3. Subsequent tests will not give valid results unless all preceding steps are passed and adjustments made.

Table 5-1. Key Sequences To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press SELECT Press C2 Press ENTER Press Step Number ^(a) Press START	Press Enter	Press REVIEW
Model 29	Press SELECT Press C1 Press START Press Step Number(a)	Press START Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number ^(a)	Press START Press START ^(a) Optional	Press BACKSPACE

For each step in the calibration procedure:

- Take measurement readings at the device sockets or test points indicated in the specific calibration procedure.
- The oscilloscope trigger point is called out on the calibration procedure photographs.
- The adjustment potentiometers on the waveform generator and the T/rise comparator card enable you to make adjustments when your measurements do not match the values in the calibration procedure; figure 5-2 shows the location of these adjustment points.
- Access each new step by pressing START (or ENTER). The new step number will appear on the display when the LogicPak is ready for the next step. To return to a previous test, press the REVIEW (or BACKSPACE) key.

Table 5-2. Error Codes

Error Code	Description	Action
21*	Illegal-Bit Error	The programmer is asked to leave intact a fuse which is already blown. Examine programmer RAM and the device's data.
22*	Programming Error	An attempt to blow a fuse was made and failed. Try the programming sequence again. If the second attempt also fails, try another device. If both devices produce this error, check the calibration of the LogicPak. If calibrated correctly, contact your local Data I/O service representative.
25*	No Socket Adapter	Insert appropriate socket adapter.
30	No (or Invalid) Device Selected	Enter valid device family and pinout codes (refer to table A-1).
31	Overcurrent	Hardware error in LogicPak or shorted device. Substitute a known-good device or consult the troubleshooting section of this manual.
32*	Backward Device/ Vcc Overcurrent	(1) Device plugged in backward; turn it around (2) Vcc overcurrent, probably caused by a faulty device.
33	Extended RAM Fail (Occurs only when PALASM adapter is installed.)	PALASM source file exceeds source buffer size.
34	Invalid Device Selected	Incorrect family and pinout codes entered. Enter proper family pinout code. This error occurs in computer remote control only.
35	Source Equation Translation Error	Check equation buffer by connecting terminal, to examine the equation buffer. This error code lets the operator know that an error exists in the source equations when the programmer is not controlled by a terminal. (Design adapters, PALASM or H & L, only.)

Error Code	Description	Action
36	Begin RAM Pointer Not = 0000	Refer to programmer manual to reset the begin RAM pointer to zero. This error usually occurs when changing from one Pak to another.
37	Invalid Device-Related Operation	Verify, program, or other illegal operation was attempted, with a design adapter installed.
38*	Calibration Step Error	(1) Indicates you have selected an incorrect calibration step, or (2) a program operation is attempted prior to exiting calibration - exit the calibration mode per the programmer manual).
63	RAM Write Error	System RAM failure. Refer to programmer manual or contact a Data I/O service representative.
65	Firmware Sum-Check Error	This indicates that the EPROM firmware in the LogicPak or adapter may have changed since the unit was shipped. Contact a Data I/O service representative.
70*	DAC Error, Vcc	Troubleshoot and repair Vcc DAC.
71*	DAC Error, Bit Switch Number 1	See subsection 4.4 of LogicPak manual.
72*	DAC Error, Bit Switch Number 2	See subsection 4.4 of LogicPak manual.
73*	DAC Error, CE	See subsection 4.4 of LogicPak manual.
74*	Logic Fingerprint Test Verify Error	Indicates one of the following Logic Fingerprint test (1) defective device. (2) Operator has entered wrong test-sum. (3) Device cannot be tested with Logic Fingerprint.
75*	Structured Test Verify Error	The device passed fuse verify but failed structured test.

CALIBRATION

Error Code	Description	Action
76	Self-Test Error	Check for a device in the socket. Remove the device and try again. If no device is in the socket, this indicates failure in the LogicPak.
77	Security Fuse	(1) Indicates that the security fuse option Programming Error cannot be programmed in the installed device, or (2) there is no security fuse option available for this type of device.
78*	No Fuse Verify Set	Indicates you have tried to program the device with the verify-option mode set for 2. The verify option will not allow this. When this error code displays, select E6 and enter 0 or 1, and then you will be allowed to program the device.
79*	Preload Not Implemented	The preload algorithm is not implemented for this device.
81	Parity Error	A parity error occurred while receiving serial data.
82	Checksum Error	Indicates an incorrect transmission of data from a peripheral to the serial port, including fuse data, CRs, STX, etc.
84	Invalid Data	
91	Fuse Address Error	

*These errors do not apply to design adapters. See LogicPak manual for locations of I/O pins.

Table 5-3. I/O Pin Error Codes

Error	I/O Pin(a)	Condition	Error	I/O Pin(a)	Condition
A0	1	Failure to read desired level on input register	D0	17	Failure to read desired TTL level on output pin
A1	2		D1	18	
A2	3		D2	19	
A3	4		D3	20	
A4	5		D4	21	
A5	6		D5	22	
A6	7		D6	23	
A7	8		D7	24	
A8	9		D8	25	
A9	10		D9	26	
AA	11		DA	27	
AB	12		DB	28	
AC	13		DC	29	
AD	14		DD	30	
AE	15		DE	31	
AF	16		DF	32	
BO	17	Failure to read desired level on input register	E0	1	Failure to read desired 10V level on desired output pin
B1	18		E1	2	
B2	19		E2	3	
B3	20		E3	4	
B4	21		E4	5	
B5	22		E5	6	
B6	23		E6	7	
B7	24		E7	8	
B8	25		E8	9	
B9	26		E9	10	
BA	27		EA	11	
BB	28		EB	12	
BC	29		EC	13	
BD	30		ED	14	
BE	31		EE	15	
BF	32		EF	16	

CALIBRATION

C0	1	Failure to read	F0	17	Failure to
C1	2	desired TTL	F1	18	read desired
C2	3	level on	F2	19	10V level on
C3	4	output pin	F3	20	desired
C4	5		F4	21	output pin
C5	6		F5	22	
C6	7		F6	23	
C7	8		F7	24	
C8	9		F8	25	
C9	10		F9	--	
CA	11		FA	27	
CB	12		FB	28	
CC	13		FC	--	
CD	14		FD	--	
CE	15		FE	--	
CF	16		FF	--	

(a) See LogicPak manual for locations of I/O pins.

6. TROUBLESHOOTING

6.1 GENERAL

This section will help you interpret and isolate failures in the LogicPak. Use it in conjunction with the calibration section, the circuit description, and the schematics provided in the back of this manual.

Three major classes of failures can occur in a system composed of a programmer and a LogicPak:

- no system operation
- poor yields
- LogicPak failure

After successfully troubleshooting and repairing the LogicPak, you must calibrate it according to the instructions in section 5. It is very important that you calibrate the programmer before you calibrate the LogicPak. Refer to your programmer manual for detailed programmer calibration procedures.

6.2 SELF-TESTING

The LogicPak performs a series of self-tests on its hardware to ensure the functionality of the module. A failure will display an error code (see table 5- 2). Because of the internal analog feedback capability in the LogicPak, voltage levels can be measured so that a "go/no-go" test can be performed. Programmable voltage levels are tested when device-related operations are executed. The TTL levels are tested when the programmer is powered up. Testing is accomplished under software control by first setting test levels and then reading back these levels through analog comparators. The comparator output levels are then verified against predetermined values.

When the programmer is powered up, the Logic Fingerprint self-test is done by testing an open socket. The LogicPak compares the open-socket test-sum against a predetermined test-sum stored in the firmware. This guarantees that all Logic Fingerprint test circuitry is functional.

6.3 EQUIPMENT SETUP

The following equipment is necessary to troubleshoot the LogicPak:

- Data I/O extender card (part number 702-1949) and service cable (part number 709-1141-002)
- one Phillips screwdriver
- one 1/16-inch Allen wrench

To prepare your LogicPak for troubleshooting, proceed as follows:

1. Turn off the programmer power (subsection 3.3).
2. Remove the LogicPak from the programmer (subsection 2.3).
3. Remove the adapter (if any) from the LogicPak.
4. Remove the four screws from the LogicPak cover (see figure 6-1).
5. Remove the two screws on each side of the LogicPak cover (see figure 6-1).
6. Lift the cover off the card cage assembly.
7. Unplug the pin driver board (701-0143-) from the bus extender board and lift it slightly until you can see the interconnect cable and its connector (figure 6-1).
8. Flip the extraction tabs out on each side of the connector (figure 6-1).
9. Pull the cable out of the connector.
10. Rotate the pin driver board 180 degrees and plug it into the connector on the front of the bus extender board (figure 6-1).

NOTE

The interconnect cable must be replaced by the extender cable before you can troubleshoot your LogicPak, as shown in figure 6-2.

11. Lift the extraction tabs on each side of the three circuit cards, as shown in figure 6-1.
12. Unplug the interconnect cable from the three connectors shown in figure 6-1 first by lifting the smaller black extraction tabs on both sides of the cable, then lifting the cable out.
13. Remove the waveform generator card along the guides as shown in figure 6-2 (the card furthest back).
14. Gently push the service extender card (702-1949) along the guides to plug it into the J2 connector on the motherboard (702-1938) where the waveform generator was located.

NOTE

Any board can now be placed on the extender board. The waveform generator card (701-1939) must be either on the extender board or in the slot just behind it.

15. Firmly, but gently, push the extender cable into the connectors on the three boards (as shown in figure 6-2). Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
16. Gently push the extender cable into the connector on the pin driver board (see figure 6-2).

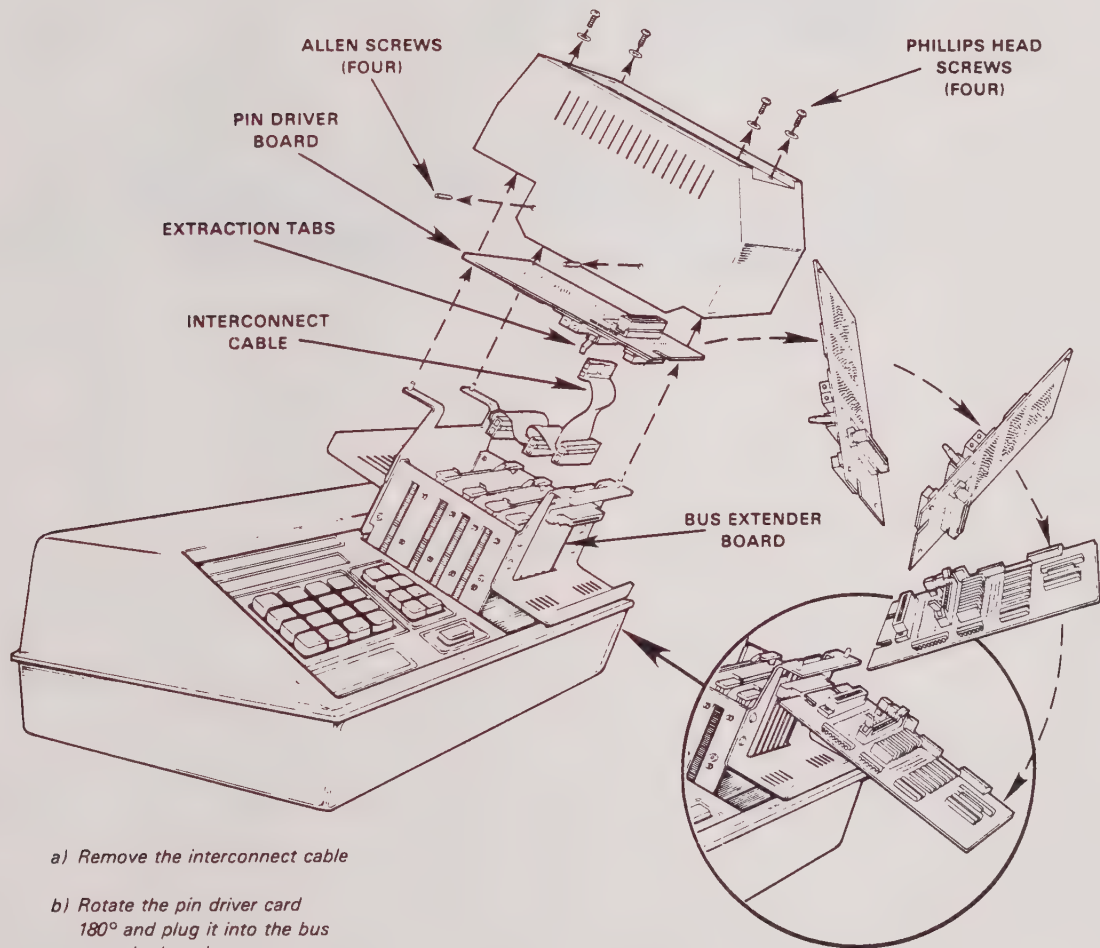


Figure 6-1. LogicPak Dissassembly

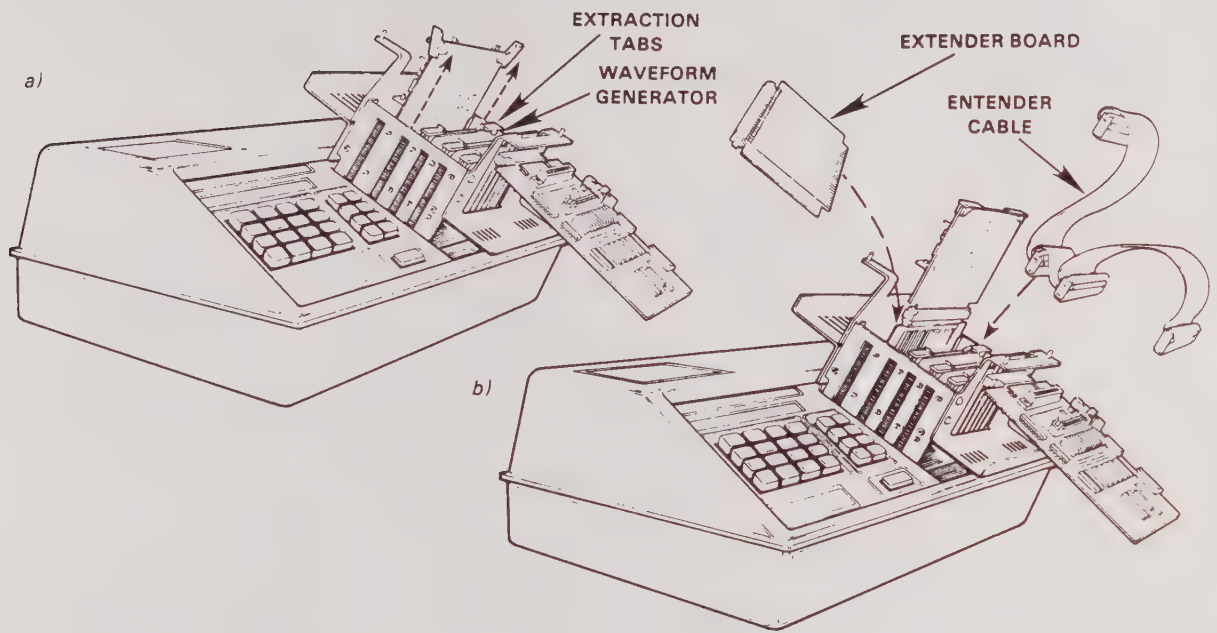


Figure 6-2. Troubleshooting Setup

APPENDIX A

CALIBRATION CHARTS

303A-001 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-001 P/T Adapter, make certain that you are using the 303A-001 Calibration Procedure.

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9	10	-0.4	0.8			
			11-20	10	-0.4	0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11	12	-0.4	0.8			
			13-24	12	-0.4	0.8			
	Pull 28-pin socket pins to TTL low	28-pin socket	1-13	14	-0.4	0.8			
			15-28	14	-0.4	0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED socket off. Confirm 24-pin socket LED socket off. Confirm 28-pin socket LED socket on.
3a	Comparator reference voltage	Waveform TP5 Generator Board (WGB) and 28-pin socket		14	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.

Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3. Remove immediately after performing test or return to test 1.)

3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
		28-pin socket	28	14	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 28 and 14.
3c	CE supply test and adjustment	28-pin socket	5	14	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 5 and 14.
3d	Bit supply switch 1 test and adjustment	28-pin socket	13	14	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 13 and 14.

APPENDIX A

Table A-1 Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
3e	Bit supply switch 2 test and adjustment	28-pin socket	1	14	19.3	19.7	19.5	NA	Connect 100-ohm/5W resistor across pins 1 and 14.
3f	DAC reference voltage	WGB and 28-pin socket	TP6	14	4.7	5.3			
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	24-pin socket LED test								Confirm that the 24- pin socket LED is on and that the 20-pin and 28-pin socket LED's are off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			2	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			17	12	3.0	5.2			
			18	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
		28-pin socket	1	14	3.0	5.2			
			3	14	3.0	5.2			
			5	14	3.0	5.2			
			7	14	3.0	5.2			
			9	14	3.0	5.2			
			11	14	3.0	5.2			
			13	14	3.0	5.2			
			16	14	3.0	5.2			
			18	14	3.0	5.2			
			21	14	3.0	5.2			
			23	14	3.0	5.2			
			25	14	3.0	5.2			
			27	14	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			18	10	-0.4	0.8			

Step	Test Name	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments		
		Location	High	Low	Min.	Max.			Nom.	
4c (cont.)		24-pin socket	3	12	-0.4	0.8				
			4	12	-0.4	0.8				
			5	12	-0.4	0.8				
			7	12	-0.4	0.8				
			9	12	-0.4	0.8				
			11	12	-0.4	0.8				
			13	12	-0.4	0.8				
			15	12	-0.4	0.8				
			19	12	-0.4	0.8				
			21	12	-0.4	0.8				
			23	12	-0.4	0.8				
			28-pin socket	2	14	-0.4	0.8			
				4	14	-0.4	0.8			
				6	14	-0.4	0.8			
		8		14	-0.4	0.8				
		10		14	-0.4	0.8				
		12		14	-0.4	0.8				
		15		14	-0.4	0.8				
		17		14	-0.4	0.8				
		19		14	-0.4	0.8				
		20		14	-0.4	0.8				
		22		14	-0.4	0.8				
		24		14	-0.4	0.8				
		26	14	-0.4	0.8					
		5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8		
					4	10	-0.4	0.8		
6	10				-0.4	0.8				
8	10				-0.4	0.8				
12	10				-0.4	0.8				
14	10				-0.4	0.8				
16	10				-0.4	0.8				
17	10				-0.4	0.8				
19	10				-0.4	0.8				
24-pin socket	1				12	-0.4	0.8			
	2				12	-0.4	0.8			
	6				12	-0.4	0.8			
	8				12	-0.4	0.8			
	10				12	-0.4	0.8			
	14			12	-0.4	0.8				
	16			12	-0.4	0.8				
	17			12	-0.4	0.8				
	18			12	-0.4	0.8				
	20			12	-0.4	0.8				
	22			12	-0.4	0.8				
	28-pin socket			1	14	-0.4	0.8			
				3	14	-0.4	0.8			
				5	14	-0.4	0.8			
7				14	-0.4	0.8				
9				14	-0.4	0.8				
11				14	-0.4	0.8				
13				14	-0.4	0.8				
16				14	-0.4	0.8				
18				14	-0.4	0.8				
21				14	-0.4	0.8				
23				14	-0.4	0.8				
25				14	-0.4	0.8				
27				14	-0.4	0.8				

APPENDIX A

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	3	12	3.0	5.2			
			4	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			13	12	3.0	5.2			
			15	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
		28-pin socket	2	14	3.0	5.2			
			4	14	3.0	5.2			
			6	14	3.0	5.2			
			8	14	3.0	5.2			
			10	14	3.0	5.2			
			12	14	3.0	5.2			
			15	14	3.0	5.2			
			17	14	3.0	5.2			
			19	14	3.0	5.2			
			20	14	3.0	5.2			
			22	14	3.0	5.2			
			24	14	3.0	5.2			
			26	14	3.0	5.2			
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.0	10.5			
			4	10	9.0	10.5			
			6	10	9.0	10.5			
			8	10	9.0	10.5			
			11	10	9.0	10.5			
			12	10	9.0	10.5			
			14	10	9.0	10.5			
			16	10	9.0	10.5			
			17	10	9.0	10.5			
			19	10	9.0	10.5			
		24-pin socket	1	12	9.0	10.5			
			2	12	9.0	10.5			
			6	12	9.0	10.5			
			8	12	9.0	10.5			
			10	12	9.0	10.5			
			13	12	9.0	10.5			
			14	12	9.0	10.5			
			16	12	9.0	10.5			
			17	12	9.0	10.5			
			18	12	9.0	10.5			
			20	12	9.0	10.5			
			22	12	9.0	10.5			

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
6a (cont.)		28-pin socket	1	14	9.0	10.5			
			3	14	9.0	10.5			
			5	14	9.0	10.5			
			7	14	9.0	10.5			
			9	14	9.0	10.5			
			11	14	9.0	10.5			
			13	14	9.0	10.5			
			16	14	9.0	10.5			
			18	14	9.0	10.5			
			19	14	9.0	10.5			
			23	14	9.0	10.5			
			25	14	9.0	10.5			
			27	14	9.0	10.5			
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	3	12	3.0	5.2			
			4	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
		28-pin socket	2	14	3.0	5.2			
			4	14	3.0	5.2			
			6	14	3.0	5.2			
			8	14	3.0	5.2			
			10	14	3.0	5.2			
			12	14	3.0	5.2			
			15	14	3.0	5.2			
			17	14	3.0	5.2			
			20	14	3.0	5.2			
			22	14	3.0	5.2			
			24	14	3.0	5.2			
			26	14	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	1.0	5.2			
			4	10	1.0	5.2			
			6	10	1.0	5.2			
			8	10	1.0	5.2			
			12	10	1.0	5.2			
			14	10	1.0	5.2			
			16	10	1.0	5.2			
			17	10	1.0	5.2			
			19	10	1.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			6	12	3.0	5.2			
			10	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			17	12	3.0	5.2			
			18	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
7a (cont.)		28-pin socket	3	14	3.0	5.2			
			5	14	3.0	5.2			
			7	14	3.0	5.2			
			11	14	3.0	5.2			
			13	14	3.0	5.2			
			16	14	3.0	5.2			
			18	14	3.0	5.2			
			21	14	3.0	5.2			
			23	14	3.0	5.2			
			25	14	3.0	5.2			
			27	14	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.0	10.5			
			3	10	9.0	10.5			
			5	10	9.0	10.5			
			7	10	9.0	10.5			
			9	10	9.0	10.5			
			11	10	9.0	10.5			
			13	10	9.0	10.5			
			15	10	9.0	10.5			
			18	10	9.0	10.5			
		24-pin socket	1	12	9.0	10.5			
			3	12	9.0	10.5			
			4	12	9.0	10.5			
			5	12	9.0	10.5			
			7	12	9.0	10.5			
			8	12	9.0	10.5			
			9	12	9.0	10.5			
			11	12	9.0	10.5			
			13	12	9.0	10.5			
			15	12	9.0	10.5			
			19	12	9.0	10.5			
			21	12	9.0	10.5			
		28-pin socket	1	14	9.0	10.5			
			2	14	9.0	10.5			
			4	14	9.0	10.5			
			6	14	9.0	10.5			
			8	14	9.0	10.5			
			9	14	9.0	10.5			
			10	14	9.0	10.5			
			12	14	9.0	10.5			
			15	14	9.0	10.5			
			17	14	9.0	10.5			
			19	14	9.0	10.5			
			20	14	9.0	10.5			
			22	14	9.0	10.5			
			24	14	9.0	10.5			
			26	14	9.0	10.5			

Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.

8	Backwards device test	28-pin socket	28	14					Connect 10-ohm/5W resistor across pins 28 and 14. Confirm error 31.
---	-----------------------	------------------	----	----	--	--	--	--	--

Steps 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

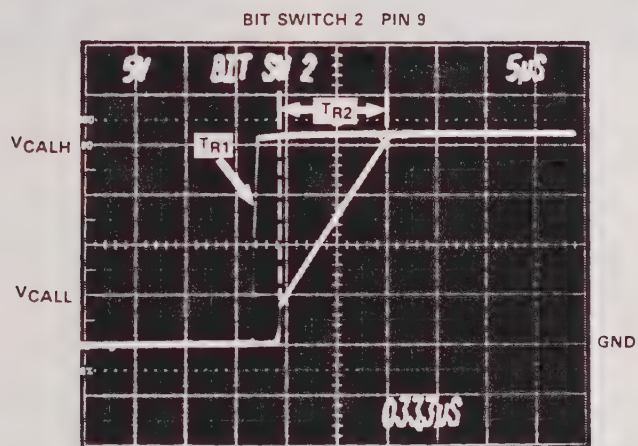
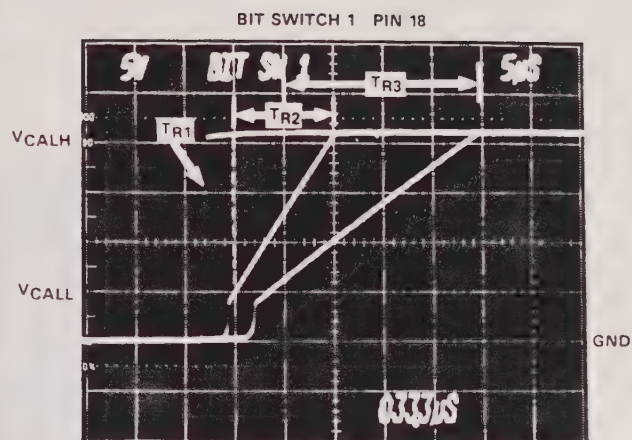
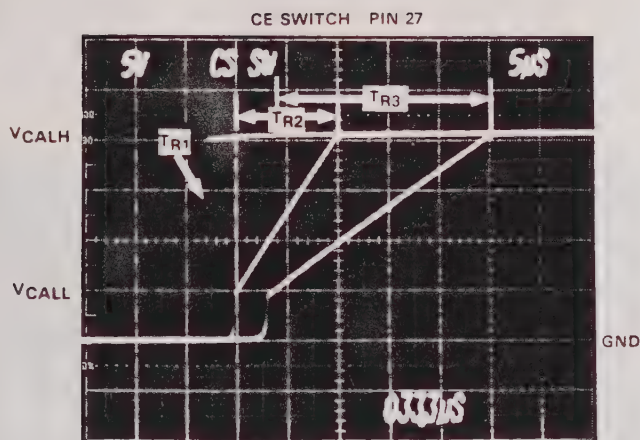
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
9	Low range over-current tests								
9a	VCC	28-pin socket	28	14					Connect 20-ohm/5W resistor across pins 28 and 14. Confirm error 31.
9b	CE switch	28-pin socket	5	14					Connect 30-ohm/5W resistor across pins 5 and 14. Confirm error 31.
9c	Bit switch 1	28-pin socket	13	14					Connect 30-ohm/5W resistor across pins 13 and 14. Confirm error 31.
9d	Bit switch 2	28-pin socket	1	14					Connect 30-ohm/5W resistor across pins 1 and 14. Confirm error 31.
10	High range over-current tests	<i>overcurrent pass with 30 Ω</i>							
10a	VCC	28-pin socket	28	14					Connect 5-ohm/5W resistor across pins 28 and 14. Confirm error 31.
10b	CE switch	28-pin socket	5	14					Connect 12-ohm/5W resistor across pins 5 and 14. Confirm error 31.
10c	Bit switch 1	28-pin socket	13	14					Connect 12-ohm/5W resistor across pins 13 and 14. Confirm error 31.
10d	Bit switch 2	28-pin socket	1	14					Connect 12-ohm/5W resistor across pins 1 and 14. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no device code has been entered. To enter the family and pinout code; Press COPY DEVICE RAM and enter a family and pinout code, for example - 9663. Press the START key.)									
12	Static programming levels tests								

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
12a	Fuse 0 (AND array)								Fuse 0 is the default fuse displayed when step 12 is selected.
	VCC supply - Vccp	28-pin socket	28	14	4.75	5.25			
	CE supply - Vix	28-pin socket	19	14	9.5	10.5			
	Bit supply - Vfeh	28-pin socket	1	14	17.0	18.0			
12b	Fuse 32 (OR array)								Enter fuse 32 at the 0000 prompt on the programmer.
	VCC supply - Vccs	28-pin socket	28	14	8.25	8.75			
	CE supply - Vfeh	28-pin socket	1	14	17.0	18.0			
	Bit supply - Vix, Vopf	28-pin socket	18	14	9.5	10.5			
12c	Fuse 1920 (output polarity)								Enter fuse 1920 at the 0000 prompt on the programmer.
	VCC supply - Vcci	28-pin socket	28	14	0.0	0.8			
	Bit supply - Voph	28-pin socket	18	14	17.0	18.0			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								
16	Rise time checks and adjustment								
	CE switch	28-pin socket	27	14	9.0us	11.0us			Adjust R1 on Rise Time Comp. for TR2 as shown on waveforms in figure A-1.
	Bit switch 1 socket	28-pin	18	14	8.0us	12.0us			
	Bit switch 2 socket	28-pin	9	14	8.0us	12.0us			

Table A-1. Calibration Procedure, LogicPak with 303A-001 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
17	Supply linearity test								
	VCC supply	28-pin socket	28	14					Verify waveforms as shown in figure A-2.
	CE supply	28-pin socket	5	14					Verify waveforms as shown in figure A-2.
	Bit supply	28-pin socket	1	14					The Bit waveforms should be linear as shown in figure A-2.

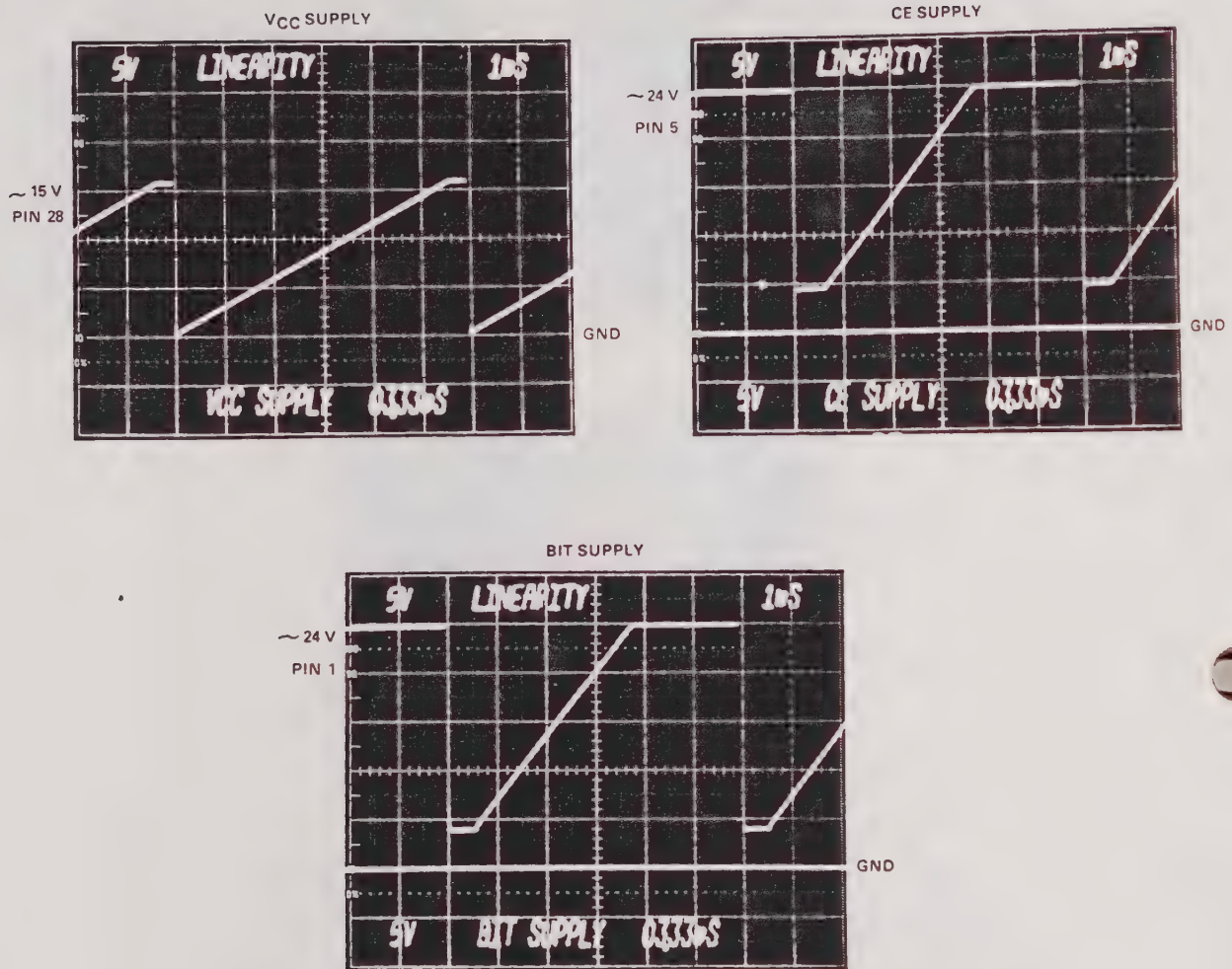


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCALH	19.0		20.5	V	Adjust R1 on 1941 card for T_{R2} CE SW as shown. Verify that others are within limits.
	VCALL	4.8		5.2	V	
	T_{R1} CE SW	0.675	0.750	0.825	μs	
	T_{R2} CE SW	9.0	10.0	11.0	μs	
	T_{R3} CE SW	15.0	20.0	25.0	μs	
	T_{R1} BIT SW	0.550	0.750	0.900	μs	
	T_{R2} BIT SW	7.0	10.0	12.0	μs	
	T_{R3} BIT SW	14.0	20.0	25.0	μs	

NOTES

- Oscilloscope trigger: TP1 on the Waveform Generator Board.
- Test points are for the 28-pin socket.

Figure A-1. 303A-001 Calibration Waveform, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 28-pin socket.

Figure A-2. 303A-001 Calibration Waveform, Step 17

303A-002 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-002 P/T Adapter, make certain that you are using the 303A-002 Calibration Procedure.

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9	10	-0.4	0.8			
			11-20	10	-0.4	0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11	12	-0.4	0.8			
			13-24	12	-0.4	0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED socket off and 24-pin socket LED socket on.
3a	Comparator reference voltage	Waveform TP5 Generator Board (WGB) & 24-pin socket		12	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test and adjustment	24-pin socket	14	12	19.6	20.4			Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB & 24-pin socket	TP6	12	4.7	5.3			

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin socket LED is off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
	Pull socket pins to TTL low	24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
5a (cont.)		24-pin socket	2	12	-0.4	0.8			
			4	12	-0.4	0.8			
			6	12	-0.4	0.8			
			8	12	-0.4	0.8			
			10	12	-0.4	0.8			
			13	12	-0.4	0.8			
			16	12	-0.4	0.8			
			18	12	-0.4	0.8			
			19	12	-0.4	0.8			
			21	12	-0.4	0.8			
			23	12	-0.4	0.8			
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			14	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.5	10.5			
			4	10	9.5	10.5			
			6	10	9.5	10.5			
			8	10	9.5	10.5			
			11	10	9.5	10.5			
			13	10	9.5	10.5			
			15	10	9.5	10.5			
			17	10	9.5	10.5			
			19	10	9.5	10.5			
		24-pin socket	2	12	9.5	10.5			
			4	12	9.5	10.5			
			6	12	9.5	10.5			
			8	12	9.5	10.5			
			10	12	9.5	10.5			
			13	12	9.5	10.5			
			14	12	9.5	10.5			
			16	12	9.5	10.5			
			18	12	9.5	10.5			
			19	12	9.5	10.5			
			21	12	9.5	10.5			
			23	12	9.5	10.5			
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			

APPENDIX A

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
6b (cont.)		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
		24-pin socket	1	12	9.5	10.5			
			3	12	9.5	10.5			
			5	12	9.5	10.5			
			7	12	9.5	10.5			
			9	12	9.5	10.5			
			11	12	9.5	10.5			
			15	12	9.5	10.5			
			17	12	9.5	10.5			
			20	12	9.5	10.5			
			22	12	9.0	10.5			

Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.)

8	Backwards device test	20-pin socket	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
		24-pin socket	24	12					Connect 10-ohm/5W resistor across pins 24 and 12. Confirm error 32.

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

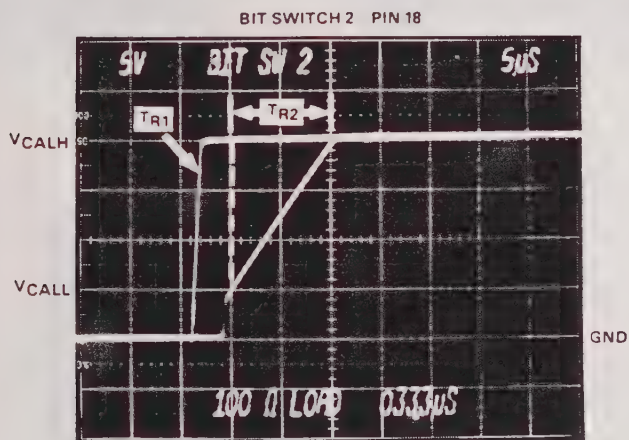
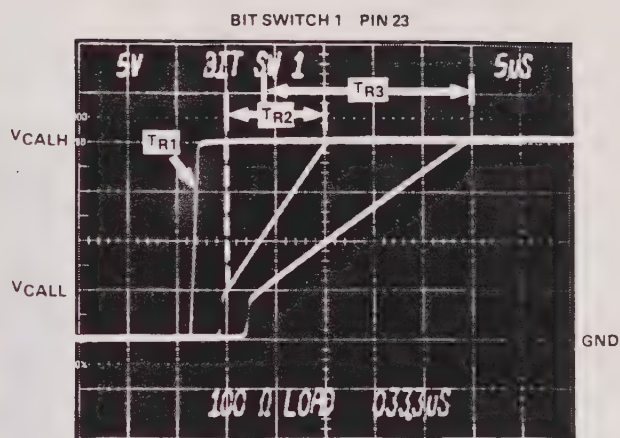
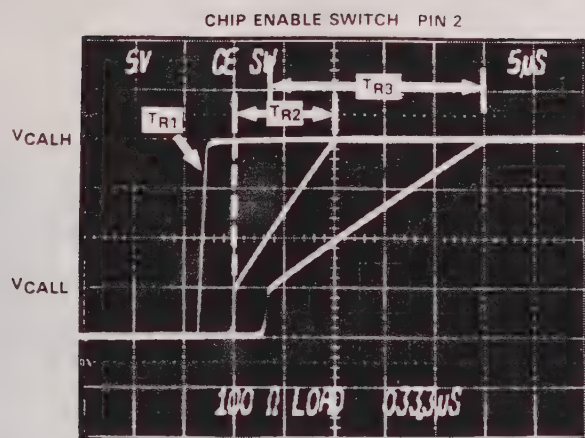
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
9	Low range over-current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 20-ohm/5W resistor across pins 24 and 12. Confirm error 31.
9b	CE switch	24-pin socket	13	12					Connect 30-ohm/5W resistor across pins 13 and 12. Confirm error 31.
9c	Bit switch 1	24-pin socket	19	12					Connect 30-ohm/5W resistor across pins 19 and 12. Confirm error 31.
9d	Bit switch 2	24-pin socket	14	12					Connect 30-ohm/5W resistor across pins 14 and 12. Confirm error 31.
10	High range tests	<i>Pass with same loads as step 9</i>							
10a	Normal-current test.	20-pin socket	20	10					Connect ~~20~~ 30-ohm/5W resistor across pins 20 and 10. Confirm no error. <i>30Ω</i>
		24-pin socket	24	12					Connect ~~20~~ 30-ohm/5W resistor across pins 24 and 12. Confirm no error. <i>30Ω</i>
		24-pin socket	13 19	12 12					Connect ~~20~~ 30-ohm/5W resistor across the 14 12 listed pins and confirm no error. <i>30Ω</i>
10b	Overcurrent test Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm error 31.
10c	Overcurrent test CE switch	24-pin socket	13	12					Connect 12-ohm/5W resistor across pins 28 and 14. Confirm error 31.

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10d	Overcurrent test Bit switch 1	24-pin socket	19	12					Connect 12-ohm/5W resistor across pins 19 and 12. Confirm error 31.
10e	Overcurrent test Bit switch 2	24-pin socket	14	12					Connect 12-ohm/5W resistor across pins 14 and 12. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM and enter a family and pinout code, for example - 9801. Press the START key.									
12	Static programming levels tests								
12a	Family code 95 and 22								Select family code 95 or 22. Enter fuse 32 at the 0000 prompt.
	VCC supply - Vccp	20-pin socket	20	10	11.5	12.0			
	CE supply - Vihh	20-pin socket	1	10	11.5	12.0			
	Bit supply - Vihh	20-pin socket	19	10	11.5	12.0			
12a	Family code 30								Select family code 30. Enter fuse 32 at the 0000 prompt.
	VCC supply - Vccp	20-pin socket	20	10	9.75	10.25			
	CE supply - Vihh	20-pin socket	1	10	9.75	10.25			
	Bit supply - Vihh	20-pin socket	19	10	9.75	10.25			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								

Table A-2. Calibration Procedure, LogicPak with 303A-002 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
16	Rise time checks and adjustment								
	CE switch	24-pin socket	2	12	9.0us	11.0us			Adjust R1 on Rise Time Comp. for TR2 as socket shown in figure A-3. Connect 100-ohm/ 5% 2W resistor across pins 2 and 12.
	Bit switch 1	24-pin socket	23	12	8.0us	12.0us			Connect 100-ohm/5% 2W resistor across pins 23 and 12.
	Bit switch 2	24-pin socket	18	12	8.0us	12.0us			Connect 100-ohm/5% 2W resistor across pins 18 and 12.
17	Supply linearity test								
	VCC supply	24-pin socket	24	12					Verify waveforms as shown in figure A-4.
	CE supply	24-pin socket	16	12					Verify waveforms as shown in figure A-4.
	Bit supply	24-pin socket	19	12					The Bit waveforms should be linear as shown in figure A-4.



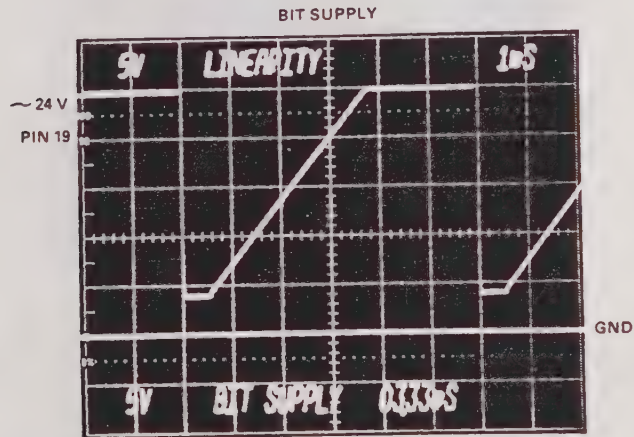
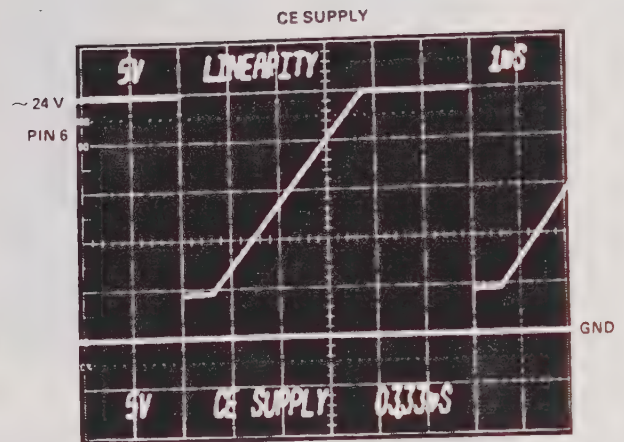
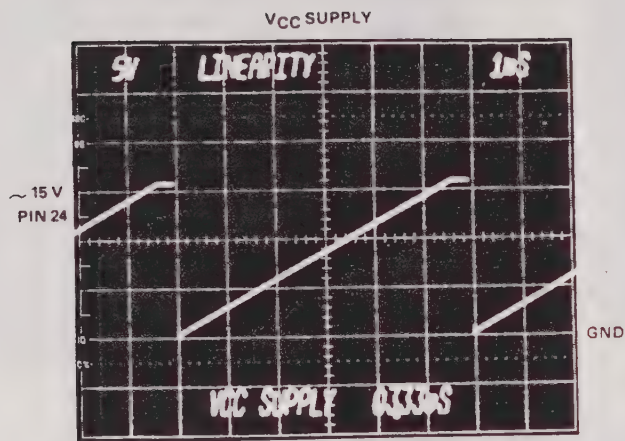
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V _{CALH}	--	20	--	V	
	V _{CALL}	--	5	--	V	
	T _{R1} CE SW	450	650	.850	μ S	Adjust R1 on 1941 card for T _{R2} CE SW as shown. Verify that others are within limits. Rise times are measured from V _{CALL} to V _{CALH} . (Voltage levels for reference only).
	T _{R2} CE SW	9.0	10.0	11.0	μ S	
	T _{R3} CE SW	15.0	20.0	25.0	μ S	
	T _{R1} BIT SW	450	650	.850	μ S	
	T _{R2} BIT SW	8.0	10.0	12.0	μ S	
	T _{R3} BIT SW	15.0	20.0	25.0	μ S	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.
3. BIT SW rise time limits are for both BIT SW1 and BIT SW2.
4. All waveforms shown loaded by 100 Ω 2W 5% resistor to ground

300mV Right

Figure A-3. 303A-002 Calibration Waveforms, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.

Figure A-4. 303A-002 Calibration Waveforms, Step 17

303A-003 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-003 P/T Adapter, make certain that you are using the 303A-003 Calibration Procedure.

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9 11-20	10 10	-0.4 -0.4	0.8 0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11 13-24	12 12	-0.4 -0.4	0.8 0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED socket off and 24-pin socket LED socket on.
3a	Comparator reference voltage	Waveform Generator Board (WGB) & 24-pin socket	TP5	12	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test	24-pin socket	14	12	19.6	20.4			Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB & 24-pin socket	TP6	12	4.7	5.4			

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin socket LED is off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
		24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			
			19	10	-0.4	0.8			

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom		
5a (cont.)		24-pin socket	2	12	-0.4	0.8			
			4	12	-0.4	0.8			
			6	12	-0.4	0.8			
			8	12	-0.4	0.8			
			10	12	-0.4	0.8			
			13	12	-0.4	0.8			
			16	12	-0.4	0.8			
			18	12	-0.4	0.8			
			19	12	-0.4	0.8			
			21	12	-0.4	0.8			
			23	12	-0.4	0.8			
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			14	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.5	10.5			
			4	10	9.5	10.5			
			6	10	9.5	10.5			
			8	10	9.5	10.5			
			11	10	9.5	10.5			
			13	10	9.5	10.5			
			15	10	9.5	10.5			
			17	10	9.5	10.5			
			19	10	9.5	10.5			
		24-pin socket	2	12	9.5	10.5			
			4	12	9.5	10.5			
			6	12	9.5	10.5			
			8	12	9.5	10.5			
			10	12	9.5	10.5			
			13	12	9.5	10.5			
			14	12	9.5	10.5			
			16	12	9.5	10.5			
			18	12	9.5	10.5			
			19	12	9.5	10.5			
			21	12	9.5	10.5			
			23	12	9.5	10.5			
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6b (cont.)		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
		24-pin socket	1	12	9.5	10.5			
			3	12	9.5	10.5			
			5	12	9.5	10.5			
			7	12	9.5	10.5			
			9	12	9.5	10.5			
			11	12	9.5	10.5			
			15	12	9.5	10.5			
			17	12	9.5	10.5			
			20	12	9.5	10.5			
			22	12	9.0	10.5			
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8. Remove immediately after performing test or return to test 1.									
8	Backwards device test socket	20-pin	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

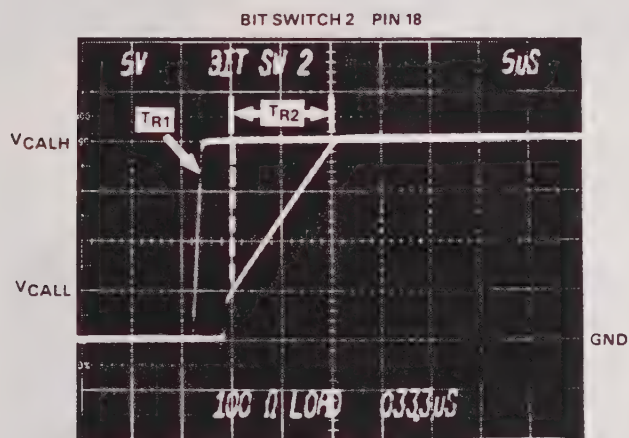
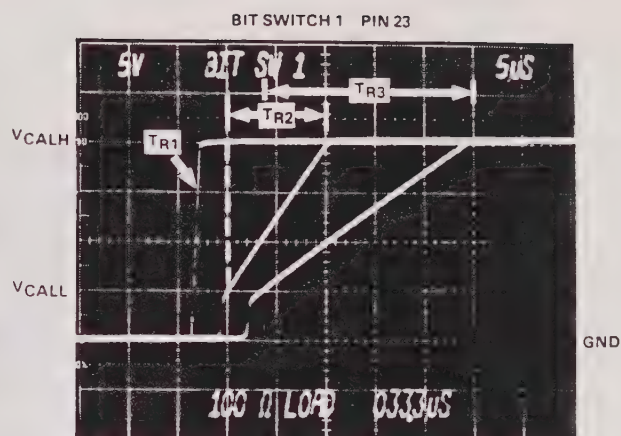
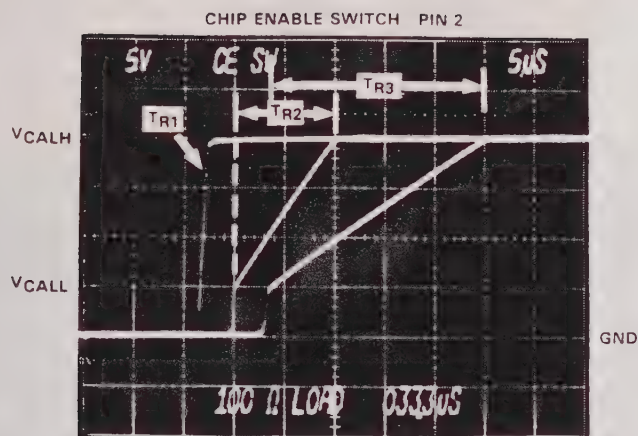
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
8 (cont.)		24-pin socket	24	12					Connect 10-ohm/5W resistor across pins 24 and 12. Confirm error 32.
(Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.)									
9	Low range over- current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 20-ohm/5W resistor across pins 24 and 12. Confirm error 31.
9b	CE switch	24-pin socket	13	12					Connect 30-ohm/5W resistor across pins 13 and 12. Confirm error 31.
9c	Bit switch 1	24-pin socket	19	12					Connect 30-ohm/5W resistor across pins
9d	Bit switch 2	24-pin socket	14	12					Connect 30-ohm/5W resistor across pins 14 and 12. Confirm error 31.
10	High range tests								
10a	Normal-current test.	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm no error. 20
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm no error. 20
		24-pin socket	13 19 14	12 12 12					Connect 12-ohm/5W resistor across the listed pins and confirm no error. 30 2
10b	Overcurrent test Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm error 31.

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10c	Overcurrent test CS switch	24-pin socket	13	12					Connect 12-ohm/5W resistor across pins 28 and 14. Confirm error 31.
10d	Overcurrent test Bit switch 1	24-pin socket	19	12					Connect 12-ohm/5W resistor across pins 19 and 12. Confirm error 31.
10e	Overcurrent test Bit switch 2	24-pin socket	14	12					Connect 12-ohm/5W resistor across pins 14 and 12. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 31 will occur if no code has been entered. To enter the family and pinout code; press COPYDEVICE RAM and enter a family and pinout code, for example - 9801. Press the START key.)									
12	Static programming levels								Select family code 98. Enter valid fuse no. at the 0000 prompt.
	VCC supply - Vcop	20-pin socket	20	10	8.25	8.75	8.50		
	Bit supply - Vopf	20-pin socket	18	10	17.0	18.0	17.5		
(The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.)									
13	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								
16	Rise time checks and adjustment								
	CE switch	24-pin	2	12	9.0us	11.0us	10.0us		Adjust R1 on Rise Time Comp. for TR2 (CE switch) in figure A-5. Connect 100-ohm, 5%, 2W resistor across the indicated pins.
	Bit switch 1	socket	23	11	9.0u	11.0u	10.0u		
	Bit switch 2		18	12	9.0u	11.0u	10.0u		

Table A-3. Calibration Procedure, LogicPak with 303A-003 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
17	Supply linearity test								
	VCC supply	24-pin	24	12					Verify waveforms as shown in figure A-6.
	CE supply	socket	6	12					
	Bit supply		19	12					

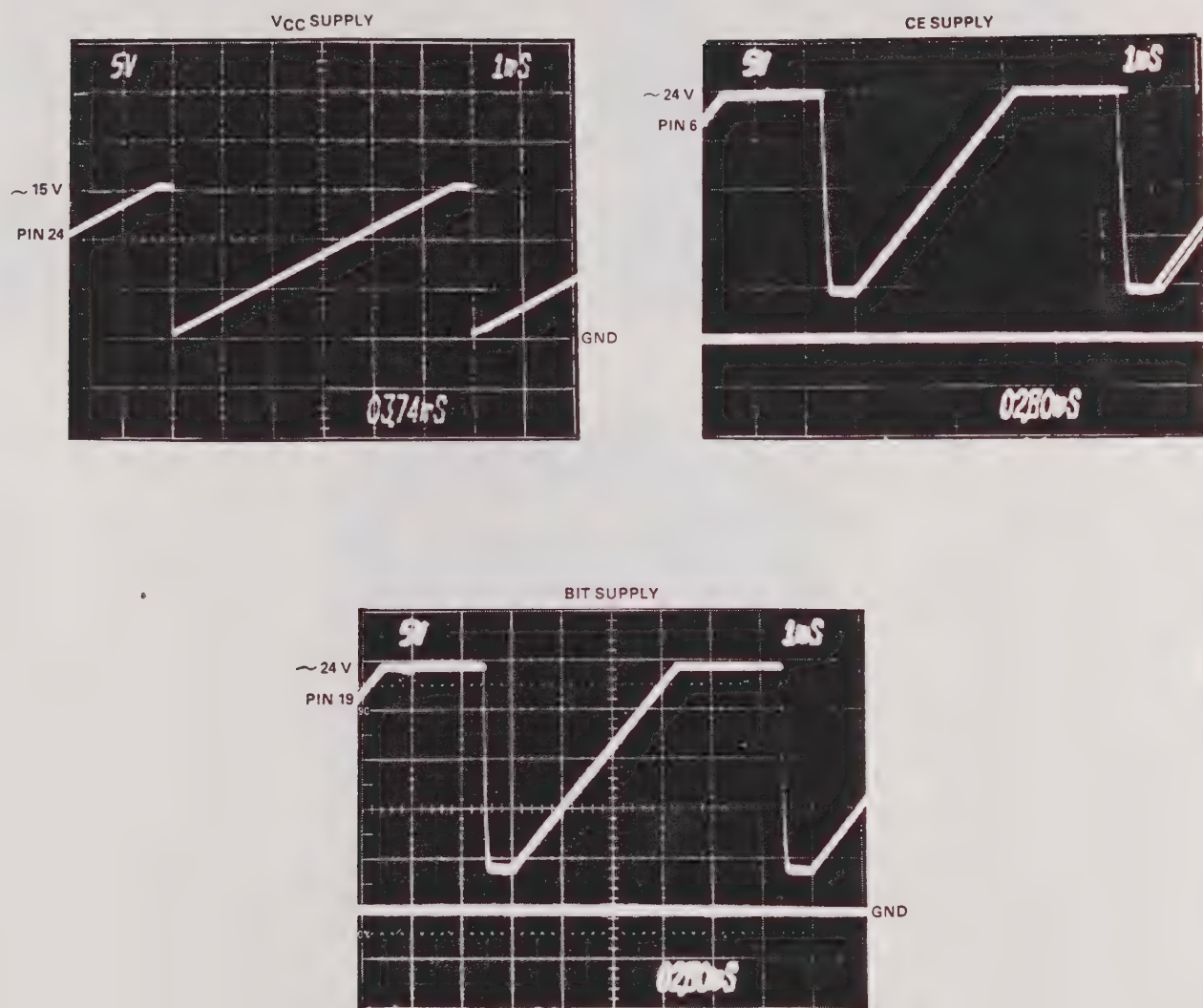


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCALH		20		V	
	VCALL		5		V	
	TR1 CE SW	450	650	850	μ S	Adjust R1 on 1941 card for TR2 CE SW as shown. Verify that others are within limits. Rise times are measured from VCALL to VCALH (Voltage levels for reference only).
	TR2 CE SW	9.0	10.0	11.0	μ S	
	TR3 CE SW	15.0	20.0	25.0	μ S	
	TR1 BIT SW	450	650	850	μ S	
	TR2 BIT SW	8.0	10.0	12.0	μ S	
	TR3 BIT SW	15.0	20.0	25.0	μ S	

NOTES

- Oscilloscope trigger: TP1 on the Waveform Generator Board.
- Test points are for the 24-pin socket.
- BIT SW rise time limits are for both BIT SW1 and BIT SW2.
- All waveforms shown loaded by 100 Ω 2W 5% to ground.

Figure A-5. 303A-003 Calibration Waveforms, Step16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.

Figure A-6. 303A-003 Calibration Waveforms, Step17

303A-004 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-004 P/T Adapter, make certain that you are using the 303A-004 Calibration Procedure.

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9	10	-0.4	0.8			
			11-20	10	-0.4	0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11	12	-0.4	0.8			
			13-24	12	-0.4	0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED socket off and 24-pin socket LED socket on.
3a	Comparator reference voltage	Waveform Generator Board (WGB) socket	TP5	12	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB. & 24-pin
Before performing step 3 through 3e insert the appropriate load resistor (after pressing the STAR key to advance to step 3) Remove immediately after performing test or return to test 1.)									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test and adjustment	24-pin socket	14	12	19.6	20.4			Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB & 24-pin socket	TP6	12	4.7	5.3			

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin socket LED is off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
		24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			

NOTE

If the programmer displays error 76 during the performance of steps 5 through 16, repeat steps 2 and 4.

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			Verify that both socket LEDs are off.
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			
			19	10	-0.4	0.8			
		24-pin socket	2	12	-0.4	0.8			
			4	12	-0.4	0.8			
			6	12	-0.4	0.8			
			8	12	-0.4	0.8			
			10	12	-0.4	0.8			
			13	12	-0.4	0.8			
			16	12	-0.4	0.8			
			18	12	-0.4	0.8			
			19	12	-0.4	0.8			
			21	12	-0.4	0.8			
			23	12	-0.4	0.8			
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			14	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.5	10.5			
			4	10	9.5	10.5			
			6	10	9.5	10.5			
			8	10	9.5	10.5			
			11	10	9.5	10.5			
			13	10	9.5	10.5			
			15	10	9.5	10.5			
			17	10	9.5	10.5			
			19	10	9.5	10.5			
		24-pin socket	2	12	9.5	10.5			
			4	12	9.5	10.5			
			6	12	9.5	10.5			
			8	12	9.5	10.5			
			10	12	9.5	10.5			
			13	12	9.5	10.5			
			14	12	9.5	10.5			
			16	12	9.5	10.5			
			18	12	9.5	10.5			
			19	12	9.5	10.5			
			21	12	9.5	10.5			
			23	12	9.5	10.5			

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
		24-pin socket	1	12	9.5	10.5			
			3	12	9.5	10.5			
			5	12	9.5	10.5			
			7	12	9.5	10.5			
			9	12	9.5	10.5			
			11	12	9.5	10.5			
			15	12	9.5	10.5			
			17	12	9.5	10.5			
			20	12	9.5	10.5			
			22	12	9.0	10.5			

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

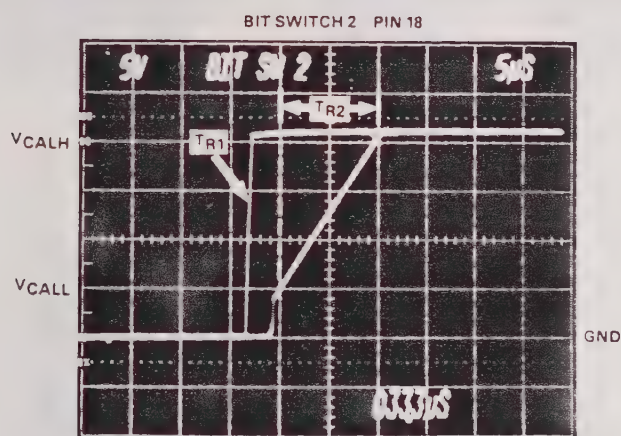
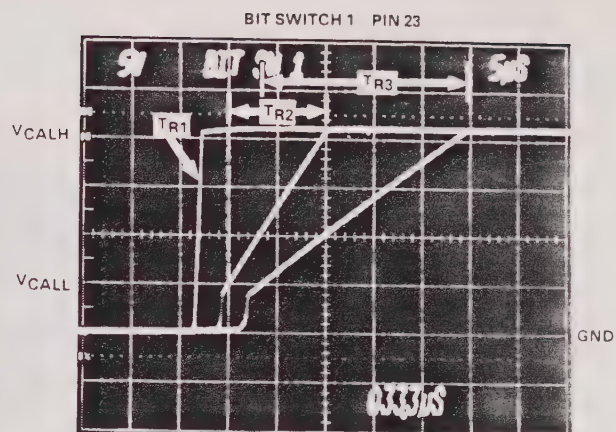
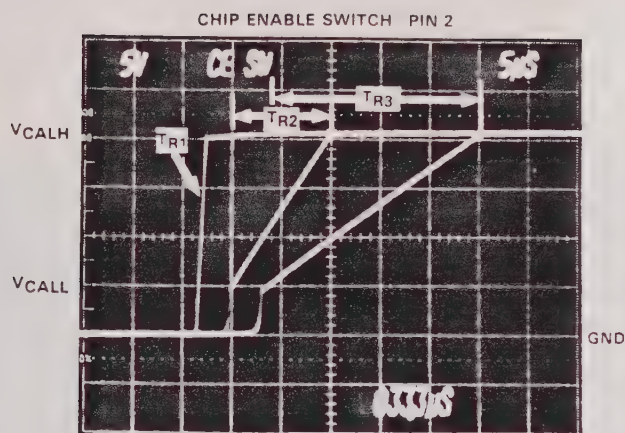
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom		
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8. Remove immediately after performing test or return to test 1.									
8	Backwards device test	20-pin socket	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
		24-pin socket	24	12					Connect 10-ohm/5W resistor across pins 24 and 12. Confirm error 32.
Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over-current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 20-ohm/5W resistor across pins 24 and 12. Confirm error 31.
9b	CE switch	24-pin socket	13	12					Connect 30-ohm/5W resistor across pins 13 and 12. Confirm error 31.
9c	Bit switch 1	24-pin socket	19	12					Connect 30-ohm/5W resistor across pins 19 and 12. Confirm error 31.
9d	Bit switch 2	24-pin socket	14	12					Connect 30-ohm/5W resistor across pins 14 and 12. Confirm error 31.
10	High range tests								
10a	Normal-current test.	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm no error.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm no error.
		24-pin socket	13 19 14	12 12 12					Connect 42-ohm/5W resistor across the listed pins and confirm no error.

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10b	Overcurrent test Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm error 31.
10c	Overcurrent test CE switch	24-pin socket	13	12					Connect 12-ohm/5W resistor across pins 28 and 14. Confirm error 31.
10d	Overcurrent test Bit switch 1	24-pin socket	19	12					Connect 12-ohm/5W resistor across pins 19 and 12. Confirm error 31.
10e	Overcurrent test Bit switch 2	24-pin socket	14	12					Connect 12-ohm/5W resistor across pins 14 and 12. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM and enter a family and pinout code, for example - 9717. Press the START key.)									
12	Static programming levels								Select family code 98. Enter valid fuse no. at the 0000 prompt.
	VCC supply - Vihh	20-pin socket	20	10	5.0	5.5			
	Bit supply - Vihh	20-pin socket	1	10	10.0	12.0			
	Bit supply - Vihh	20-pin socket	19	10	17.0	18.0			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, program- ming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, program- ming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								

Table A-4. Calibration Procedure, LogicPak with 303A-004 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
16	Rise time checks and adjustment								
	CE switch	24-pin	2	12	9.0us	11.0us	10.0us		Adjust R1 on Rise Time Comp. (for CE switch) for TR2 in figure A-7. Connect 100-ohm, 5%, 2W resistor across the indicated pins.
	Bit switch 1	socket	23	12	8.0us	12.0us			
	Bit switch 2		18	12	8.0us	12.0us			
17	Supply linearity test								
	VCC supply	24-pin	24	12					Verify waveforms as shown in figure A-8.
	CE supply	socket	6	12					
	Bit supply		19	12					

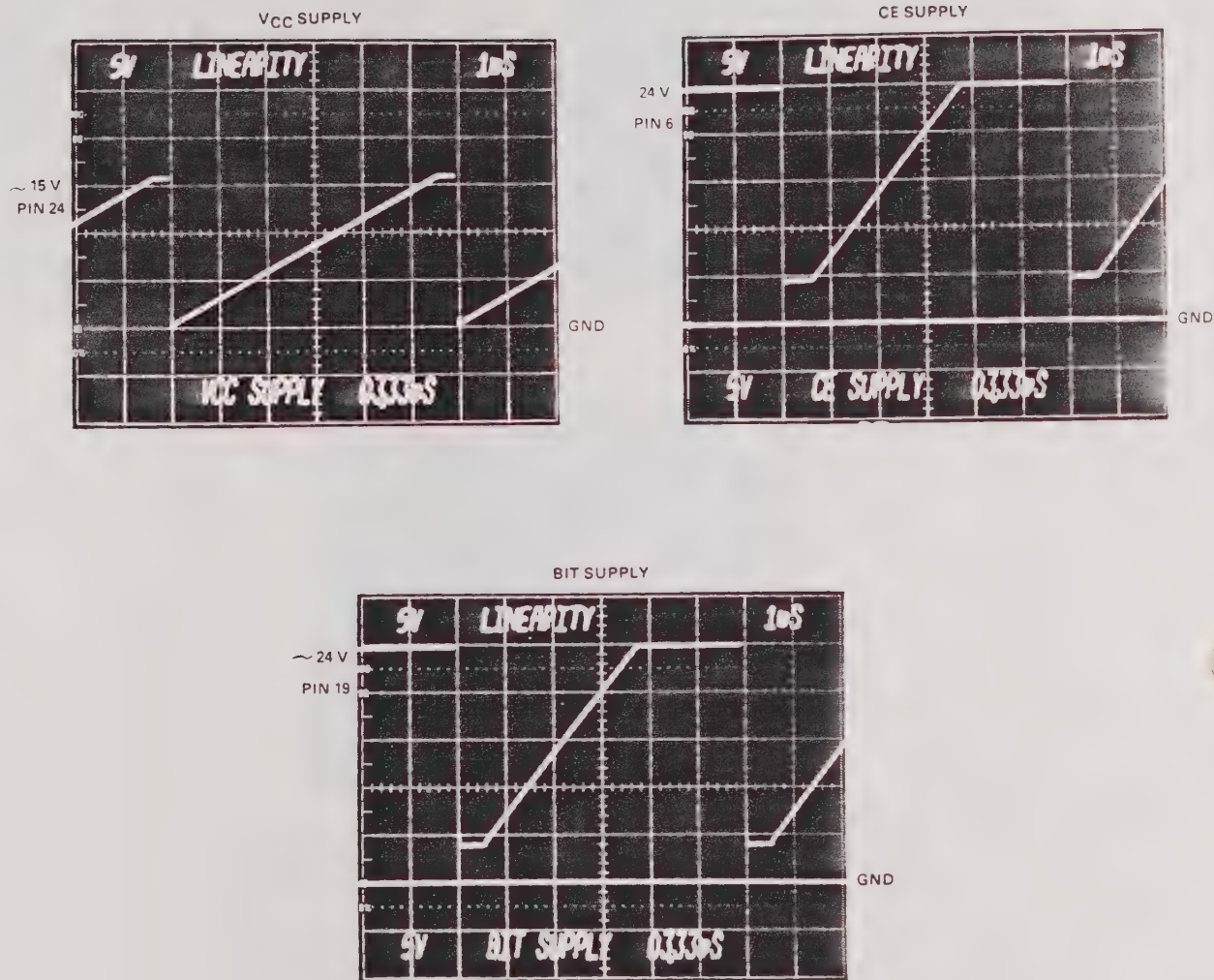


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VcalH	-	20	-	V	Adjust R1 on 1941 card for TR2 CE SW as shown. Verify that others are within limits. Rise times are measured from VCALL to VcalH. (Voltage levels for reference only.)
	VCALL	-	5	-	V	
	TR1 CE SW	450	650	850	μ s	
	TR2 CE SW	9.0	10.0	11.0	μ s	
	TR3 CE SW	15.0	20.0	25.0	μ s	
	TR1 BIT SW	450	650	850	μ s	
	TR2 BIT SW	8.0	10.0	12.0	μ s	
	TR3 BIT SW	15.0	20.0	25.0	μ s	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.
3. BIT SW rise time limits are for both BIT SW1 and BIT SW2.
4. All waveforms shown loaded by $100\ \Omega$ 2W 5% to ground.

Figure A-7. 303A-004 Calibration Waveforms, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.

Figure A-8. 303A-004 Calibration Waveforms, Step 17

303A-006 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-006 P/T Adapter, make certain that you are using the 303A-006 Calibration Procedure.

Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9 11-20	10 10	-0.4 -0.4	0.8 0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11 13-24	12 12	-0.4 -0.4	0.8 0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED socket off and 24-pin socket LED socket on.
3a	Comparator reference voltage test and adjustment	Waveform Generator Board (WGB) & 24-pin socket	TP5	12	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test	24-pin socket	14	12	19.6	20.4			Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB & 24-pin socket	TP6	14	4.7	5.3			

Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin socket LED is off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
		24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			

NOTE

If the programmer displays error 76 during the performance of steps 5 through 16, repeat steps 2 and 4.

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Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
		24-pin socket	1	12	9.5	10.5			
			3	12	9.5	10.5			
			5	12	9.5	10.5			
			7	12	9.5	10.5			
			9	12	9.5	10.5			
			11	12	9.5	10.5			
			15	12	9.5	10.5			
			17	12	9.5	10.5			
			20	12	9.5	10.5			
			22	12	9.0	10.5			

Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

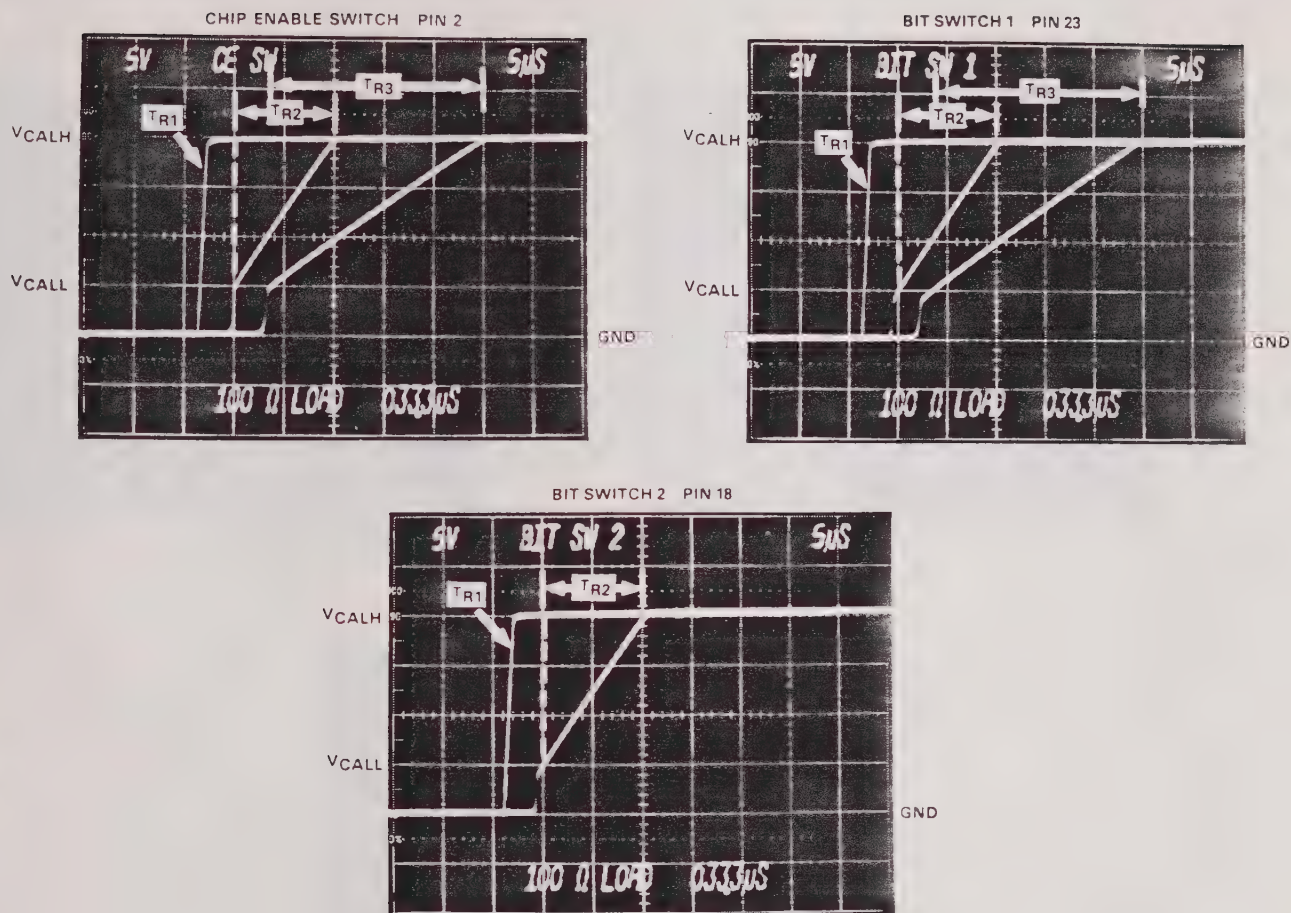
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.									
8	Backwards device test	20-pin socket	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
		24-pin socket	24	12					Connect 10-ohm/5W resistor across pins 24 and 12. Confirm error 32.
Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over-current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 20-ohm/5W resistor across pins 24 and 12. Confirm error 31.
9b	CE switch	24-pin socket	13	12					Connect 30-ohm/5W resistor across pins 13 and 12. Confirm error 31.
9c	Bit switch 1	24-pin socket	19	12					Connect 30-ohm/5W resistor across pins 19 and 12. Confirm error 31.
9d	Bit switch 2	24-pin socket	14	12					Connect 30-ohm/5W resistor across pins 14 and 12. Confirm error 31.
10	High range tests								
10a	Normal-current test	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm no error.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm no error.

Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10b	Overcurrent test Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm error 31.
10c	Overcurrent test CS switch	24-pin socket	13	12					Connect 12-ohm/5W resistor across pins 13 and 12. Confirm error 31.
10d	Overcurrent test Bit switch 1	24-pin socket	19	12					Connect 12-ohm/5W resistor across pins 19 and 12. Confirm error 31.
10e	Overcurrent test Bit switch 2	24-pin socket	14	12					Connect 12-ohm/5W resistor across pins 14 and 12. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM and enter a family and pinout code, for example - 9917. Press the START key.									
12	Static programming levels								Select family code 98. Enter fuse 0 at the 0000 prompt.
	VCC supply - Vihh	20-pin socket	20	10	10.25	10.75			
	Bit supply - Vihh	20-pin socket	1	10	10.25	10.75			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may used to verify active programming signals.
14	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								

Table A-5. Calibration Procedure, LogicPak with 303A-006 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
16	Rise time checks and adjustment								
	CE switch	24-pin	2	12	9.0us	11.0us	10.0us		Adjust R1 on Rise Time Comp for TR2 as shown in figure A-9 (for CE switch). Connect 100-ohm, 5%, 2W resistor across the indicated pins.
	Bit switch 1	socket	23	12	8.0us	12.0us			
	Bit switch 2		18	12	8.0us	12.0us			
17	Supply linearity test								
	VCC supply	24-pin	24	12					Verify waveforms as shown in figure A-10.
	CE supply	socket	6	12					
	BIT supply		19	12					

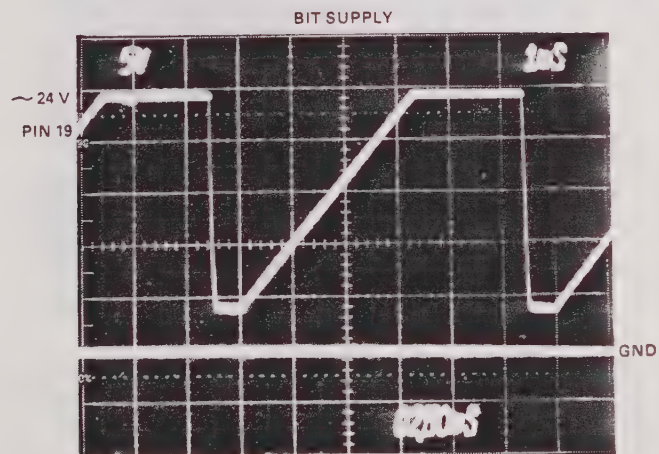
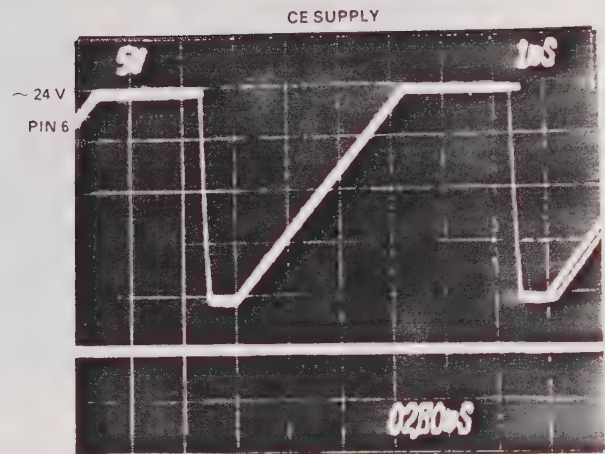
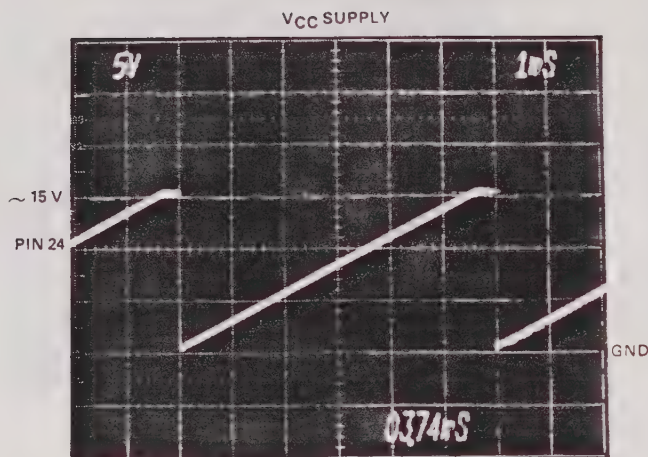


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VcalH	--	20	--	V	Adjust R1 on 1941 card for TR2 CE SW as shown. Verify that others are within limits. Rise times are measured from Vcall to VcalH. (Voltage levels for reference only).
	Vcall	--	5	--	V	
	TR1 CE SW	450	650	850	μ S	
	TR2 CE SW	9.0	10.0	11.0	μ S	
	TR3 CE SW	15.0	20.0	25.0	μ S	
	TR1 BIT SW	450	650	850	μ S	
	TR2 BIT SW	8.0	10.0	12.0	μ S	
	TR3 BIT SW	15.0	20.0	25.0	μ S	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.
3. BIT SW rise time limits are for both BIT SW1 and BIT SW2
4. All waveforms shown loaded by 100 Ω 2W 5% resistor to ground.

Figure A-9. 303A-006 Calibration Waveforms, Step16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board
2. Test points are for the 24-pin socket.

Figure A-10. 303A-006 Calibration Waveforms, Step17

303A-007 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-007 P/T Adapter, make certain that you are using the 303A-007 Calibration Procedure.

Table A-6. Calibration Procedure, LogicPak with 303A-007 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull socket pins to TTL low	20-pin socket	2-9 12-20 1,11	10 10 10	-0.4 -0.4 0.0	0.8 0.8 1.0			
CAUTION									
Do not leave programmer unattended in calibration mode beyond step 1.									
2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm LED on.
3a	Comparator reference voltage test and adjustment	Waveform TP5 10 Generator Board (WGB) & 20-pin socket	10.20	10.28	10.24			R28/WGB	Waveform Generator Board is abbreviated as WGB.
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
3c	CE supply test and adjustment	20-pin socket	1	10	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 1 and 10.
3d	Bit supply test and adjustment	WGB & 20-pin socket	TP2	10	20.6	21.0	20.8	R6/WGB	
3e	DAC reference voltage	WGB & 20-pin socket	TP6	10	4.7	5.3			
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Pull socket pins to TTL high	20-pin socket	2 4 6 8 13 15 17 19	10 10 10 10 10 10 10 10	3.0 3.0 3.0 3.0 3.0 3.0 3.0 3.0	5.2 5.2 5.2 5.2 5.2 5.2 5.2 5.2			

Table A-6. Calibration Procedure, LogicPak with 303A-007 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4b	Pull socket pins to TTL low	20-pin socket	3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
4c	Verify pins 1 and 11	20-pin	1	10	0.0	1.2			
			11	10	0.0	1.2			

NOTE

If the programmer displays error 76 during the performance of steps 5 through 16, repeat steps 2 and 4.

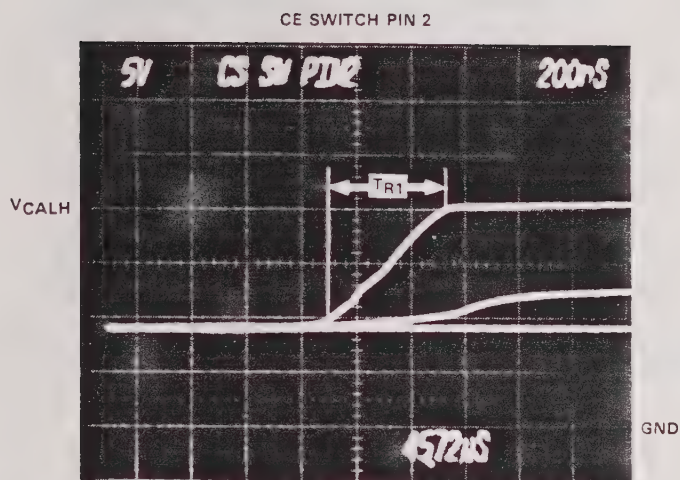
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			Verify that socket LED is off.
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			
			19	10	-0.4	0.8			
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.5	10.5			
			4	10	9.5	10.5			
			6	10	9.5	10.5			
			8	10	9.5	10.5			
			11	10	9.5	10.5			
			13	10	9.5	10.5			
			15	10	9.5	10.5			
			17	10	9.5	10.5			
6b	Pull socket pins to TTL high socket	20-pin	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			

Table A-6. Calibration Procedure, LogicPak with 303A-007 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.									
8	Backwards device test	20-pin socket	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over- current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
9b	CE switch	20-pin socket	1	10					Connect 30-ohm/5W resistor across pins 1 and 10. Confirm error 31.
10	High range tests								
10a	Normal-current test	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm no error.
		20-pin socket	1	10					Connect 30-ohm/5W resistor across pins 1 and 10. Confirm no error.
10b	Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.

Table A-6. Calibration Procedure, LogicPak with 303A-007 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10c	CE switch	20-pin socket	1	10					Connect 12-ohm 5W resistor across pins 1 and 10. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM and enter a family and pinout code, for example - 2417. Press the START key.)									
12	Static programming levels								Select family code 24. Enter fuse 2016 at the 0000 prompt.
	VCC supply - Vccp	20-pin socket	20	10	11.5	12.5			
	CE supply - Vihp	20-pin socket	1	10	(Vccp -2V)		Vccp		Vccp is established in previous measure- ment.
			9	10	(Vccp -2V)		Vccp		
			19	10	(Vccp -2V)		Vccp		
			11	10	-5.5	-6.5	-6.0		
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								
16	Rise time checks and adjustment								
	CE switch	20-pin	2	10					Adjust R1 on Rise Time Comp. for TR2 as shown in figure A-11 (for CE switch). Connect 100-ohm, 5%, 2W resistor across the indicated pins.
17	Supply linearity test								
	VCC supply	20-pin socket	20	10					Verify waveforms as shown in figure A-12.
	CE supply		1	10					

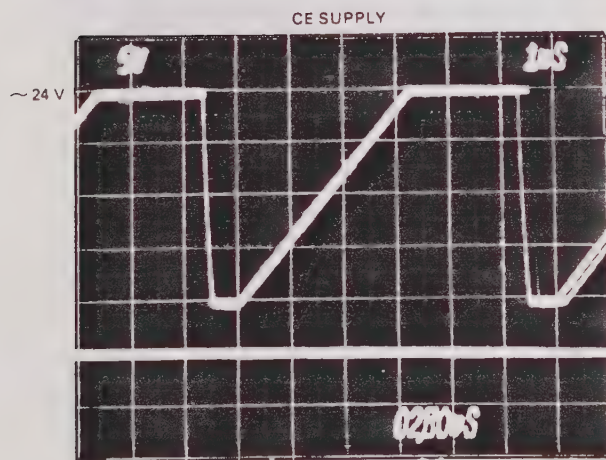
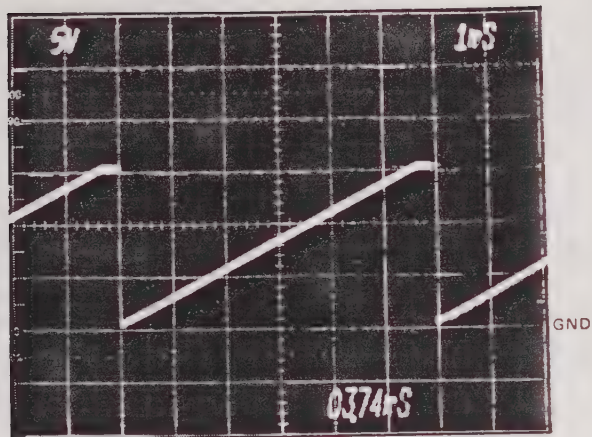


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V _{CALH}	19.8	-	20.2	V	Time measured from 10V to V _{CALH} . Adjust R1 on 1941 card.
	T _{R1} CE SW	200	400	.600	μs	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 20-pin socket.

Figure A-11. 303A-007 Calibration Waveforms, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 20-pin socket.

Figure A-12. 303A-007 Calibration Waveforms, Step 17

303A-008 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-008 P/T Adapter, make certain that you are using the 303A-008 Calibration Procedure.

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
1	Pull socket pins to TTL low	40-pin socket	1-29 31-40	10 10	-0.4 -0.4	0.8 0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm LED on.
3a	Comparator reference voltage test and adjustment	Waveform TP5 10 Generator Board (WGB) & 40-pin socket			10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.

Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.

3b	VCC supply test and adjustment	40-pin socket	10	30	11.90	12.10	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 10 and 30.
3c	CE supply test and adjustment	40-pin socket	24	30	11.90	12.10	12.0	R31/WGB	Connect 240-ohm/2W resistor across pins 24 and 30.
3d	Bit supply switch 1 test and adjustment	40-pin socket	4	30	11.90	12.10	12.0	R6/WGB	Connect 240-ohm/2W resistor across pins 4 and 30.
3e	Bit supply switch 2 test and adjustment	40-pin socket	25	30	11.90	12.10	12.0	R6/WGB	Connect 240-ohm/2W resistor across pins 25 and 30.
3f	LC supply test	40-pin socket	29	30	11.90	12.50	12.0		Connect 1K-ohm/2W resistor across pins 29 and 30.
3g	DAC reference voltage	WGB & 40-pin socket	TP6	30	4.7	5.3			
3h	DC to DC supply test and adjustment	40-pin socket	9	30	19.90	20.10	20.0	R22 (see fig. 3-1)	Connect 470-ohm/2W resistor across pins 25 and 30.

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Pull socket pins to TTL high	40-pin socket	1	30	3.0	5.2			
			3	30	3.0	5.2			
			5	30	3.0	5.2			
			6	30	3.0	5.2			
			8	30	3.0	5.2			
			11	30	3.0	5.2			
			13	30	3.0	5.2			
			16	30	3.0	5.2			
			17	30	3.0	5.2			
			19	30	3.0	5.2			
			21	30	3.0	5.2			
			23	30	3.0	5.2			
			25	30	3.0	5.2			
			26	30	3.0	5.2			
			28	30	3.0	5.2			
			31	30	3.0	5.2			
			33	30	3.0	5.2			
			37	30	3.0	5.2			
			39	30	3.0	5.2			
4b	Pull socket pins to TTL low	40-pin socket	2	30	-0.4	0.8			
			4	30	-0.4	0.8			
			7	30	-0.4	0.8			
			9	30	-0.4	0.8			
			12	30	-0.4	0.8			
			14	30	-0.4	0.8			
			15	30	-0.4	0.8			
			18	30	-0.4	0.8			
			20	30	-0.4	0.8			
			22	30	-0.4	0.8			
			24	30	-0.4	0.8			
			27	30	-0.4	0.8			
			29	30	-0.4	0.8			
			32	30	-0.4	0.8			
			34	30	-0.4	0.8			
			35	30	-0.4	0.8			
			36	30	-0.4	0.8			
			38	30	-0.4	0.8			
			40	30	-0.4	0.8			

NOTE

If the programmer displays error 76 during the performance of steps 5 through 16, repeat steps 2 and 4.

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
5a	Pull socket pins to TTL high	40-pin socket	2	30	3.0	5.2			
			4	30	3.0	5.2			
			7	30	3.0	5.2			
			9	30	3.0	5.2			
			12	30	3.0	5.2			
			14	30	3.0	5.2			
			15	30	3.0	5.2			
			18	30	3.0	5.2			
			20	30	3.0	5.2			
			22	30	3.0	5.2			
			24	30	3.0	5.2			
			27	30	3.0	5.2			
			29	30	3.0	5.2			
			32	30	3.0	5.2			
			34	30	3.0	5.2			
			35	30	3.0	5.2			
			36	30	3.0	5.2			
			38	30	3.0	5.2			
			40	30	3.0	5.2			
5b	Pull socket pins to TTL low	40-pin socket	1	30	-0.4	0.8			
			3	30	-0.4	0.8			
			5	30	-0.4	0.8			
			6	30	-0.4	0.8			
			8	30	-0.4	0.8			
			11	30	-0.4	0.8			
			13	30	-0.4	0.8			
			16	30	-0.4	0.8			
			17	30	-0.4	0.8			
			19	30	-0.4	0.8			
			21	30	-0.4	0.8			
			23	30	-0.4	0.8			
			25	30	-0.4	0.8			
			26	30	-0.4	0.8			
			28	30	-0.4	0.8			
			31	30	-0.4	0.8			
			33	30	-0.4	0.8			
			37	30	-0.4	0.8			
			39	30	-0.4	0.8			
6a	Pull socket pins to source voltage	40-pin socket	1	30	9.50	10.50	10.00		
			3	30	9.50	10.50	10.00		
			5	30	9.50	10.50	10.00		
			6	30	9.50	10.50	10.00		
			8	30	9.50	10.50	10.00		
			11	30	9.50	10.50	10.00		
			13	30	9.50	10.50	10.00		
			15	30	9.50	10.50	10.00		
			16	30	9.50	10.50	10.00		
			17	30	9.50	10.50	10.00		
			19	30	9.50	10.50	10.00		
			21	30	9.50	10.50	10.00		
			23	30	9.50	10.50	10.00		
			26	30	9.50	10.50	10.00		
			28	30	9.50	10.50	10.00		
			31	30	9.50	10.50	10.00		
			33	30	9.50	10.50	10.00		
			37	30	9.50	10.50	10.00		
			39	30	9.50	10.50	10.00		

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

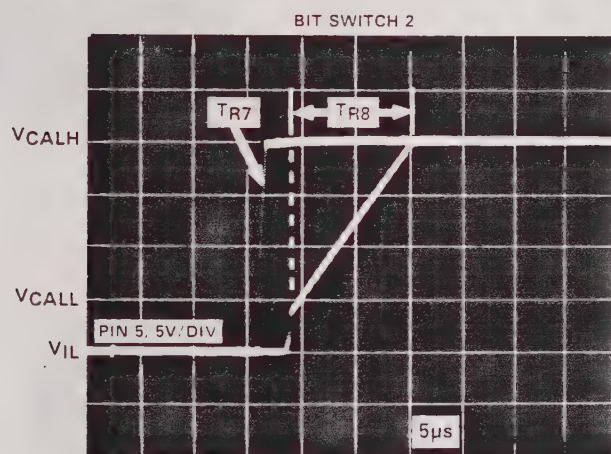
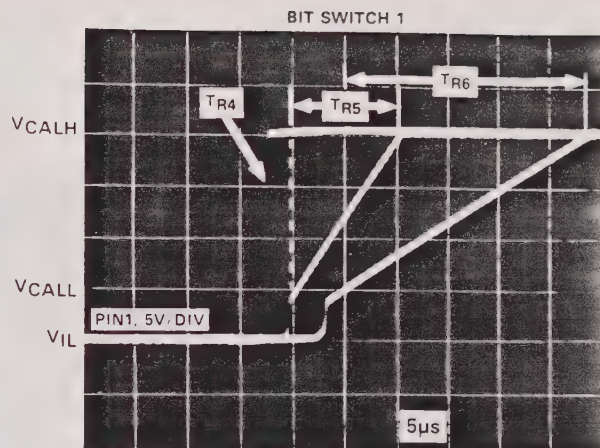
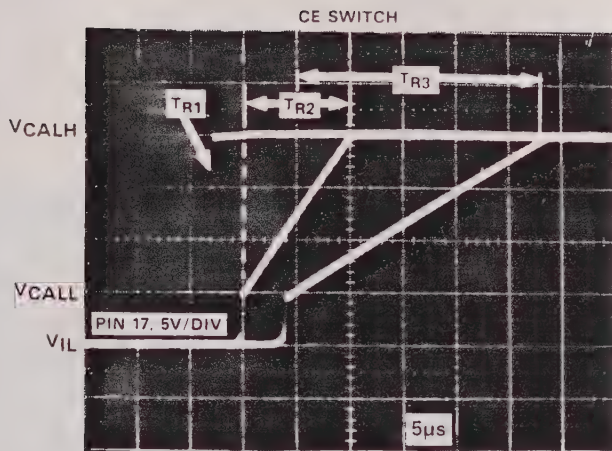
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6b	Pull socket pins to TTL high	40-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			18	10	3.0	5.2			
			20	10	3.0	5.2			
			22	10	3.0	5.2			
			24	10	3.0	5.2			
			25	10	3.0	5.2			
			27	10	3.0	5.2			
			29	10	3.0	5.2			
			32	10	3.0	5.2			
			34	10	3.0	5.2			
			35	10	3.0	5.2			
			36	10	3.0	5.2			
			38	10	3.0	5.2			
			40	10	3.0	5.2			
7a	Pull socket pins to source voltage	40-pin socket	2	10	9.50	10.50	10.00		
			4	10	9.50	10.50	10.00		
			6	10	9.50	10.50	10.00		
			7	10	9.50	10.50	10.00		
			12	10	9.50	10.50	10.00		
			14	10	9.50	10.50	10.00		
			18	10	9.50	10.50	10.00		
			20	10	9.50	10.50	10.00		
			22	10	9.50	10.50	10.00		
			24	10	9.50	10.50	10.00		
			25	10	9.50	10.50	10.00		
			26	10	9.50	10.50	10.00		
			27	10	9.50	10.50	10.00		
			29	10	9.50	10.50	10.00		
			32	10	9.50	10.50	10.00		
			34	10	9.50	10.50	10.00		
			35	10	9.50	10.50	10.00		
			36	10	9.50	10.50	10.00		
			38	10	9.50	10.50	10.00		
			40	10	9.50	10.50	10.00		
7b	Pull socket pins to TTL high	40-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	30	3.0	5.2			
			8	30	3.0	5.2			
			11	30	3.0	5.2			
			13	30	3.0	5.2			
			15	30	3.0	5.2			
			16	30	3.0	5.2			
			17	30	3.0	5.2			
			19	30	3.0	5.2			
			21	30	3.0	5.2			
			23	30	3.0	5.2			
			28	30	3.0	5.2			
			31	30	3.0	5.2			
			33	30	3.0	5.2			
			37	30	3.0	5.2			
			39	30	3.0	5.2			

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.									
8a	Backwards device test	40-pin socket	10	30					Connect 10-ohm, 1/4W resistor across pins 10 and 30. Confirm error 32.
8b	Backwards device test	40-pin socket	40	30					Connect 10-ohm, 1/4W resistor across pins 40 and 30. Confirm error 32.
Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over-current tests								
9a	VCC	40-pin socket	10	30					Connect 15-ohm/5W resistor across pins 10 and 30. Confirm error 31.
9b	CE switch	40-pin socket	24	30					Connect 22-ohm/2W resistor across pins 24 and 30. Confirm error 31.
9c	Bit switch 1	40-pin socket	4	30					Connect 22-ohm/2W resistor across pins 4 and 30. Confirm error 31.
9d	Bit switch 2	40-pin socket	25	30					Connect 22-ohm/2W resistor across pins 25 and 30. Confirm error 31.
10	High range over-current tests								
10a	VCC	40-pin socket	10	30					Connect 5-ohm/5W resistor across pins 10 and 30. Confirm error 31.
10b	CE switch	40-pin socket	24	30					Connect 10-ohm/2W resistor across pins 24 and 30. Confirm error 31.
10c	Bit switch 1	40-pin socket	4	30					Connect 10-ohm/2W resistor across pins 4 and 30. Confirm error 31.
10d	Bit switch 2	40-pin socket	25	30					Connect 10-ohm/2W resistor across pins 25 and 30. Confirm error 31.

Table A-7. Calibration Procedure, LogicPak with 303A-008 P/T Adapter

Step	Test Name	Location	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
			High	Low	Min.	Max.	Nom.		
11	Skip this step; not used for calibration								
12	Static programming levels								If levels are incorrect, perform adjustment per step 3, or repair the Pak.
	VCC supply - Vccp	40-pin socket	10	30	11.5	12.0	11.75		
	CE supply - Vihh	40-pin socket	15	30	11.5	12.0	11.75		
	Bit supply - Vihh	40-pin socket	5	30	11.5	12.0	11.75		
	DC supply	40-pin socket	29	30	19.5	20.5	20.0		
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals.
15	This step is not used.								
16	Rise time checks and adjustment								Adjust R1 on Time Rise Comp. for TR2 in figure A-13 (for CE switch). Connect 100-ohm, 5%, 2W resistor across the indicated pins.
	CE switch	40-pin socket	17	30					
	Bit switch 1		1	30					
	Bit switch 2		5	30					
17	Supply linearity test								Verify waveforms as shown in figure A-14.
	VCC supply	40-pin socket	10	30					
	CE supply		24	30					
	Bit switch 2		25	30					

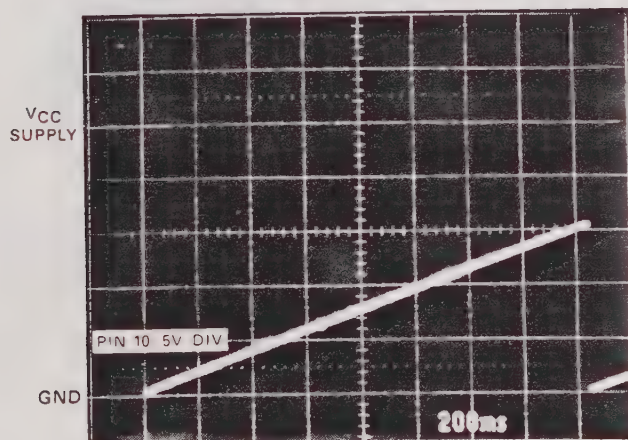
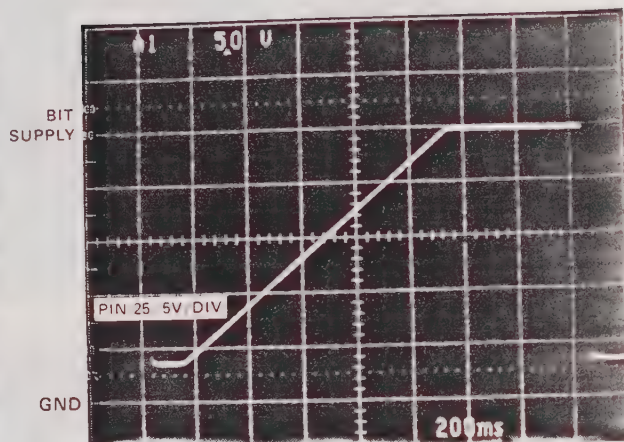
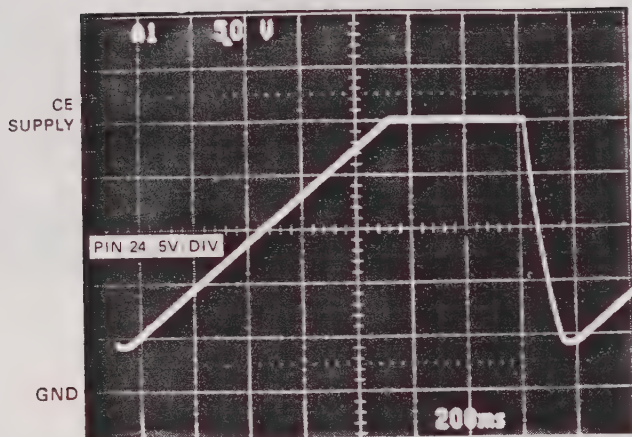


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
RISE TIME	TR1	.450	650	850	µs	Adjust R1 on 1941 card for TR1, TR2 and TR3. Verify that TR4 - TR8 are within .µmits
	TR2	9.0	10.0	11.0	µs	
	TR3	15.0	20.0	25.0	µs	
	TR4	.450	650	850	µs	
	TR5, TR7	8.0	10.0	12.0	µs	
	TR6, TR8	15.0	20.0	25.0	µs	
	VCALL		5.0		V	
	VCALH		20.0		V	
	VIL	0.4		0.8	V	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 40-pin socket
3. Risetimes measured from VCALL to VCALH (Voltage levels are for reference only.)
4. Delay time base may be required - horizontal position is insignificant

Figure A-13. 303A-008 Calibration Waveforms, Step 16



NOTES

1. Trigger on falling edge.
2. Verify linear positive slope.

Figure A-14. 303A-008 Calibration Waveforms, Step 17

303A-009 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-009 P/T Adapter, make certain that you are using the 303A-009 Calibration Procedure.

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9 11-20	10 10	-0.4 -0.4	0.8 0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11 13-24	12 12	-0.4 -0.4	0.8 0.8			
CAUTION									
Do not leave programmer unattended in calibration mode beyond step 1.									
2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED off and 24-pin socket LED on.
3a	Comparator reference voltage test and adjustment	Waveform Generator Board (WGB) & 24-pin socket	TP5	12	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key). Remove immediately after performing test or return to test 1.									
3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test	24-pin socket	14	12	19.6	20.4			Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB & 24-pin socket	TP6	12	4.7	5.3			

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	Socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin socket LED is off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
		24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			

NOTE

If the programmer displays error 76 during the performance of steps 5 through 16, repeat steps 2 and 4.

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			
			19	10	-0.4	0.8			
			24-pin socket	2	12	-0.4	0.8		
		4		12	-0.4	0.8			
		6		12	-0.4	0.8			
		8		12	-0.4	0.8			
		10		12	-0.4	0.8			
		13		12	-0.4	0.8			
		16		12	-0.4	0.8			
		18		12	-0.4	0.8			
		19		12	-0.4	0.8			
		21		12	-0.4	0.8			
		23	12	-0.4	0.8				
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
			24-pin socket	1	12	3.0	5.2		
		3		12	3.0	5.2			
		5		12	3.0	5.2			
		7		12	3.0	5.2			
		9		12	3.0	5.2			
		11		12	3.0	5.2			
		14		12	3.0	5.2			
		15		12	3.0	5.2			
		17		12	3.0	5.2			
		20		12	3.0	5.2			
		22	12	3.0	5.2				
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.5	10.5			
			4	10	9.5	10.5			
			6	10	9.5	10.5			
			8	10	9.5	10.5			
			11	10	9.5	10.5			
			13	10	9.5	10.5			
			15	10	9.5	10.5			
			17	10	9.5	10.5			
			19	10	9.5	10.5			
			24-pin socket	2	12	9.5	10.5		
		4		12	9.5	10.5			
		6		12	9.5	10.5			
		8		12	9.5	10.5			
		10		12	9.5	10.5			
		13		12	9.5	10.5			
		14		12	9.5	10.5			
		16		12	9.5	10.5			
		18		12	9.5	10.5			
		19		12	9.5	10.5			
		21	12	9.5	10.5				
23	12	9.5	10.5						

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
7a	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.5	10.5			
			3	10	9.5	10.5			
			5	10	9.5	10.5			
			7	10	9.5	10.5			
			9	10	9.5	10.5			
			12	10	9.5	10.5			
			14	10	9.5	10.5			
			16	10	9.5	10.5			
			18	10	9.5	10.5			
		24-pin socket	1	12	9.5	10.5			
			3	12	9.5	10.5			
			5	12	9.5	10.5			
			7	12	9.5	10.5			
			9	12	9.5	10.5			
			11	12	9.5	10.5			
			15	12	9.5	10.5			
			17	12	9.5	10.5			
			20	12	9.5	10.5			
			22	12	9.0	10.5			

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

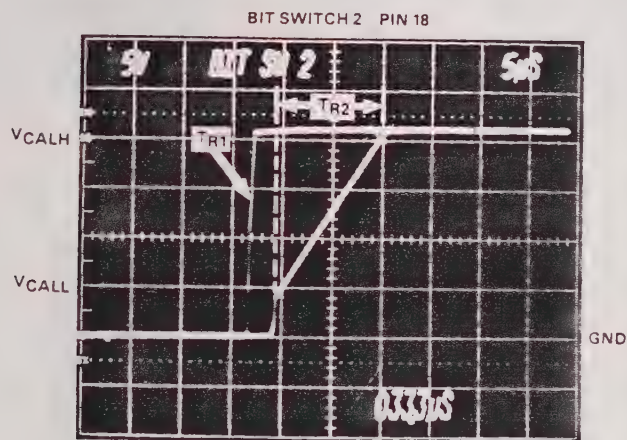
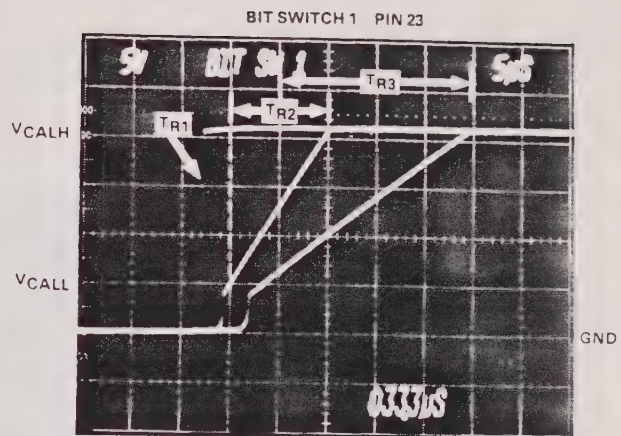
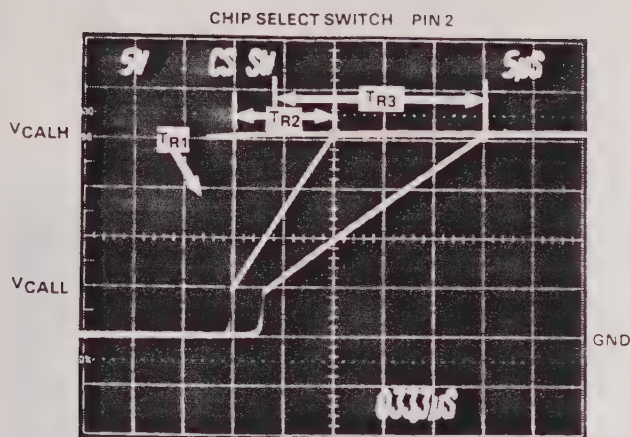
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comment
		Location	High	Low	Min.	Max.	Nom.		
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8. Remove immediately after performing test or return to test 1.									
8	Backwards device test	20-pin socket	20	10					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
		24-pin socket	24	12					Connect 10-ohm/5W resistor across pins 20 and 10. Confirm error 32.
Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over-current tests								
9a	VCC	20-pin socket	20	10					Connect 20-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 20-ohm/5W resistor across pins 24 and 12. Confirm error 31.
9b	CE switch	24-pin socket	13	12					Connect 30-ohm/5W resistor across pins 13 and 12. Confirm error
9c	Bit switch 1	24-pin socket	19	12					Connect 30-ohm/5W resistor across pins 19 and 12. Confirm error 31.
9d	Bit switch 2	24-pin socket	14	12					Connect 30-ohm/5W resistor across pins 14 and 12. Confirm error 31.
10	High range tests								
10a	Normal-current test.	20-pin socket	20	10					Connect ~~5-ohm~~ 5W resistor across pins 20 and 10. Confirm no error.
		24-pin socket	24	12					Connect ~~5-ohm~~ 5W resistor across pins 24 and 12. Confirm no error.

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom		
10b	Overcurrent test Vcc	20-pin socket	20	10					Connect 5-ohm/5W resistor across pins 20 and 10. Confirm error 31.
		24-pin socket	24	12					Connect 5-ohm/5W resistor across pins 24 and 12. Confirm error 31.
10c	Overcurrent test CS switch	24-pin socket	13	12					Connect 12-ohm/5W resistor across pins 13 and 12. Confirm error 31.
10d	Overcurrent test Bit switch 1	24-pin socket	19	12					Connect 12-ohm/5W resistor across pins 19 and 12. Confirm error 31.
10e	Overcurrent test Bit switch 2	24-pin socket	14	12					Connect 12-ohm/5W resistor across pins 14 and 12. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM and enter a family and pinout code, for example - 9717. Press the START key.)									
12	Static programming levels								Select family/pinout code 2230.
	VCC supply - Vihh	20-pin socket	20	10	4.75	5.25			
	CS supply	20-pin socket	13	10	14.75	15.25			
	Bit supply	20-pin socket	1	10	20.75	21.25			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming signals.
14	Optional waveform observation, prog- ramming algorithm								Not necessary for calibration - may be used to verify active programming
15	This step is not used.								

Table A-8. Calibration Procedure, LogicPak with 303A-009 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
16	Rise time checks and adjustment								
	CE switch	24-pin	2	12	9.0us	11.0us	10.0us		Adjust R1 on Time Rise Comp. for TR2 in figure A-15 (CE switch). Connect 100-ohm, 5%, 2W resistor across the indicated pins.
	Bit switch 1	socket	23	12	8.0us	12.0us			
	Bit switch 2		18	12	8.0us	12.0us			
17	Supply linearity test								
	VCC supply	24-pin	24	12					Verify waveforms as shown in figure A-16.
	CE supply	socket	16	12					
	BIT supply		19	12					

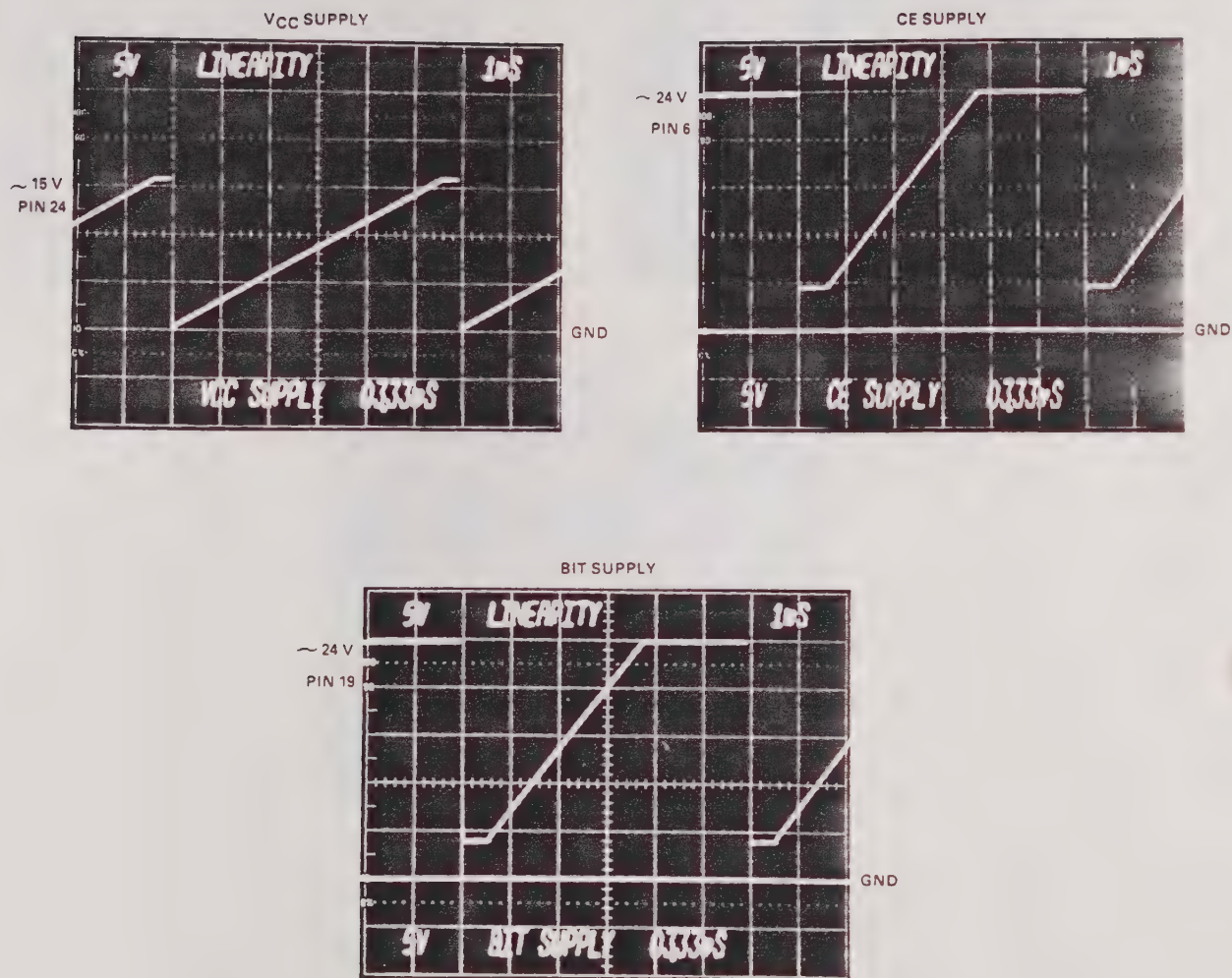


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V _{CALH}	19.8		20.2	V	Adjust R1 on 1941 card for TR2 CS SW as shown. Verify that others are within limits
	V _{CALL}	4.8		5.2	V	
	TR1 CE SW	0.675	0.750	0.825	µs	
	TR2 CS SW	9.0	10.0	11.0	µs	
	TR3 CS SW	15.0	20.0	25.0	µs	
	TR1 BIT SW	0.600	0.750	0.900	µs	
	TR2 BIT SW	8.0	10.0	12.0	µs	
	TR3 BIT SW	12.5	20.0	25.0	µs	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board
2. Test points are for the 24-pin socket.

Figure A-15. 303A-009 Calibration Waveforms, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 24-pin socket.

Figure A-16. 303A-009 Calibration Waveforms, Step 17

303A-010 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-010 P/T Adapter, make certain that you are using the 303A-010 Calibration Procedure.

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 40-pin socket pins to TTL low	40-pin socket	1-19	20	-0.4	0.8			
			21-40	20	-0.4	0.8			
	Pull 44-pin socket pins to TTL low	44-pin socket	1-21	22	-0.4	0.8			
			23-44	22	-0.4	0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are 9F-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm LED off.
3a	Comparator reference voltage	Waveform TP5 Generator Board (WGB) and 40-pin socket		20	10.20	10.28	10.24	R28/WGB	Waveform Generator Board is abbreviated as WGB.

Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3). Remove immediately after performing test or return to test 1.

3b	VCC supply test and adjustment	40-pin socket	40	20	11.3	11.5	11.4	R9/WGB	Connect 50-ohm/5W resistor across pins 40 and 20.
		44-pin socket	1	22	11.3	11.5	11.4	R9/WGB	Connect 50-ohm/5W resistor across pins 1 and 22.
3c	CE supply test and adjustment	40-pin socket	11	20	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 11 and 20.
3d	Bit supply switch 1 test and adjustment	40-pin socket	5	20	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 5 and 20.
3e	Bit supply switch 2 test and adjustment	40-pin socket	1	20	19.6	20.4			Connect 100-ohm/5W resistor across pins 1 and 20.
3f	DAC reference voltage	WGB and 40-pin socket	TP6	20	4.7	5.3			

4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
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Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4a	Socket LED test								Confirm that the LED is on.
4b	Pull socket pins to TTLhigh	40-pin socket	1	20	3.0	5.2			
			2	20	3.0	5.2			
			4	20	3.0	5.2			
			5	20	3.0	5.2			
			7	20	3.0	5.2			
			9	20	3.0	5.2			
			11	20	3.0	5.2			
			14	20	3.0	5.2			
			15	20	3.0	5.2			
			17	20	3.0	5.2			
			18	20	3.0	5.2			
			21	20	3.0	5.2			
			22	20	3.0	5.2			
			24	20	3.0	5.2			
			25	20	3.0	5.2			
			27	20	3.0	5.2			
			29	20	3.0	5.2			
			31	20	3.0	5.2			
			33	20	3.0	5.2			
			36	20	3.0	5.2			
		44-pin socket	2	22	3.0	5.2			
			3	22	3.0	5.2			
			5	22	3.0	5.2			
			6	22	3.0	5.2			
			8	22	3.0	5.2			
			10	22	3.0	5.2			
			12	22	3.0	5.2			
			15	22	3.0	5.2			
			16	22	3.0	5.2			
			19	22	3.0	5.2			
			20	22	3.0	5.2			
			24	22	3.0	5.2			
			25	22	3.0	5.2			
			27	22	3.0	5.2			
			28	22	3.0	5.2			
			30	22	3.0	5.2			
			32	22	3.0	5.2			
			34	22	3.0	5.2			
			36	22	3.0	5.2			
			40	22	3.0	5.2			
4c	Pull socket pins to TTL low	40-pin socket	3	20	-0.4	0.8			
			6	20	-0.4	0.8			
			8	20	-0.4	0.8			
			10	20	-0.4	0.8			
			12	20	-0.4	0.8			
			13	20	-0.4	0.8			
			16	20	-0.4	0.8			
			19	20	-0.4	0.8			
			23	20	-0.4	0.8			
			26	20	-0.4	0.8			
			28	20	-0.4	0.8			
			30	20	-0.4	0.8			
			32	20	-0.4	0.8			
			34	20	-0.4	0.8			
			35	20	-0.4	0.8			
			37	20	-0.4	0.8			
			38	20	-0.4	0.8			
			39	20	-0.4	0.8			

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4c (cont.)		44-pin socket	4	22	-0.4	0.8			
			7	22	-0.4	0.8			
			9	22	-0.4	0.8			
			11	22	-0.4	0.8			
			13	22	-0.4	0.8			
			14	22	-0.4	0.8			
			18	22	-0.4	0.8			
			21	22	-0.4	0.8			
			26	22	-0.4	0.8			
			29	22	-0.4	0.8			
			31	22	-0.4	0.8			
			33	22	-0.4	0.8			
			35	22	-0.4	0.8			
			37	22	-0.4	0.8			
			38	22	-0.4	0.8			
			41	22	-0.4	0.8			
			42	22	-0.4	0.8			
			43	22	-0.4	0.8			
5a	Pull socket pins to TTL low	40-pin socket	1	20	-0.4	0.8			
			2	20	-0.4	0.8			
			4	20	-0.4	0.8			
			5	20	-0.4	0.8			
			7	20	-0.4	0.8			
			9	20	-0.4	0.8			
			11	20	-0.4	0.8			
			14	20	-0.4	0.8			
			15	20	-0.4	0.8			
			17	20	-0.4	0.8			
			18	20	-0.4	0.8			
			21	20	-0.4	0.8			
			22	20	-0.4	0.8			
			24	20	-0.4	0.8			
			25	20	-0.4	0.8			
			27	20	-0.4	0.8			
			29	20	-0.4	0.8			
			31	20	-0.4	0.8			
			33	20	-0.4	0.8			
			36	20	-0.4	0.8			
		44-pin socket	2	22	-0.4	0.8			
			3	22	-0.4	0.8			
			5	22	-0.4	0.8			
			6	22	-0.4	0.8			
			8	22	-0.4	0.8			
			10	22	-0.4	0.8			
			12	22	-0.4	0.8			
			15	22	-0.4	0.8			
			16	22	-0.4	0.8			
			19	22	-0.4	0.8			
			20	22	-0.4	0.8			
			24	22	-0.4	0.8			
			25	22	-0.4	0.8			
			27	22	-0.4	0.8			
			28	22	-0.4	0.8			
			30	22	-0.4	0.8			
			32	22	-0.4	0.8			
			34	22	-0.4	0.8			
			36	22	-0.4	0.8			
			40	22	-0.4	0.8			

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
5b	Pull socket pins to TTL high	40-pin socket	3	20	3.0	5.2			
			6	20	3.0	5.2			
			8	20	3.0	5.2			
			10	20	3.0	5.2			
			12	20	3.0	5.2			
			13	20	3.0	5.2			
			16	20	3.0	5.2			
			19	20	3.0	5.2			
			23	20	3.0	5.2			
			26	20	3.0	5.2			
			28	20	3.0	5.2			
			30	20	3.0	5.2			
			32	20	3.0	5.2			
			34	20	3.0	5.2			
			35	20	3.0	5.2			
			37	20	3.0	5.2			
			38	20	3.0	5.2			
			39	20	3.0	5.2			
		44-pin socket	4	22	3.0	5.2			
			7	22	3.0	5.2			
			9	22	3.0	5.2			
			11	22	3.0	5.2			
			13	22	3.0	5.2			
			14	22	3.0	5.2			
			18	22	3.0	5.2			
			21	22	3.0	5.2			
			26	22	3.0	5.2			
			29	22	3.0	5.2			
			31	22	3.0	5.2			
			33	22	3.0	5.2			
			35	22	3.0	5.2			
			37	22	3.0	5.2			
			38	22	3.0	5.2			
			41	22	3.0	5.2			
			42	22	3.0	5.2			
			43	22	3.0	5.2			
6a	Pull socket pins to source voltage	40-pin socket	1	20	9.5	10.5			
			2	20	9.5	10.5			
			4	20	9.5	10.5			
			5	20	9.5	10.5			
			7	20	9.5	10.5			
			9	20	9.5	10.5			
			11	20	9.5	10.5			
			14	20	9.5	10.5			
			15	20	9.5	10.5			
			17	20	9.5	10.5			
			18	20	9.5	10.5			
			21	20	9.5	10.5			
			22	20	9.5	10.5			
			24	20	9.5	10.5			
			33	20	9.5	10.5			
			36	20	9.5	10.5			

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6a (cont.)		44-pin socket	2	22	3.0	5.2			
			3	22	3.0	5.2			
			5	22	3.0	5.2			
			6	22	3.0	5.2			
			8	22	3.0	5.2			
			10	22	3.0	5.2			
			12	22	3.0	5.2			
			15	22	3.0	5.2			
			16	22	3.0	5.2			
			19	22	3.0	5.2			
			20	22	3.0	5.2			
			24	22	3.0	5.2			
			25	22	3.0	5.2			
			27	22	3.0	5.2			
			36	22	3.0	5.2			
			40	22	3.0	5.2			
6b	Pull socket pins to TTL high	40-pin socket	3	20	3.0	5.2			
			6	20	3.0	5.2			
			8	20	3.0	5.2			
			10	20	3.0	5.2			
			12	20	3.0	5.2			
			13	20	3.0	5.2			
			16	20	3.0	5.2			
			19	20	3.0	5.2			
			23	20	3.0	5.2			
			25	20	3.0	5.2			
			26	20	3.0	5.2			
			27	20	3.0	5.2			
			28	20	3.0	5.2			
			29	20	3.0	5.2			
			30	20	3.0	5.2			
			31	20	3.0	5.2			
			32	20	3.0	5.2			
			34	20	3.0	5.2			
			35	20	3.0	5.2			
			37	20	3.0	5.2			
			38	20	3.0	5.2			
			39	20	3.0	5.2			
		44-pin socket	4	22	-0.4	0.8			
			7	22	-0.4	0.8			
			9	22	-0.4	0.8			
			11	22	-0.4	0.8			
			13	22	-0.4	0.8			
			14	22	-0.4	0.8			
			18	22	-0.4	0.8			
			21	22	-0.4	0.8			
			26	22	-0.4	0.8			
			28	22	-0.4	0.8			
			29	22	-0.4	0.8			
			30	22	-0.4	0.8			
			31	22	-0.4	0.8			
			32	22	-0.4	0.8			
			33	22	-0.4	0.8			
			34	22	-0.4	0.8			
			35	22	-0.4	0.8			
			37	22	-0.4	0.8			
			38	22	-0.4	0.8			
			41	22	-0.4	0.8			
			42	22	-0.4	0.8			
			43	22	-0.4	0.8			

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
7a	Pull socket pins to TTL high	40-pin socket	1	20	3.0	5.2			
			2	20	3.0	5.2			
			4	20	3.0	5.2			
			5	20	3.0	5.2			
			7	20	3.0	5.2			
			9	20	3.0	5.2			
			11	20	3.0	5.2			
			14	20	3.0	5.2			
			15	20	3.0	5.2			
			17	20	3.0	5.2			
			18	20	3.0	5.2			
			21	20	3.0	5.2			
			22	20	3.0	5.2			
			24	20	3.0	5.2			
			25	20	3.0	5.2			
			26	20	3.0	5.2			
			27	20	3.0	5.2			
			28	20	3.0	5.2			
			29	20	3.0	5.2			
			30	20	3.0	5.2			
			31	20	3.0	5.2			
			32	20	3.0	5.2			
			33	20	3.0	5.2			
			36	20	3.0	5.2			
		44-pin socket	2	22	3.0	5.2			
			3	22	3.0	5.2			
			5	22	3.0	5.2			
			6	22	3.0	5.2			
			8	22	3.0	5.2			
			10	22	3.0	5.2			
			12	22	3.0	5.2			
			15	22	3.0	5.2			
			16	22	3.0	5.2			
			19	22	3.0	5.2			
			20	22	3.0	5.2			
			24	22	3.0	5.2			
			25	22	3.0	5.2			
			27	22	3.0	5.2			
			28	22	3.0	5.2			
			30	22	3.0	5.2			
			32	22	3.0	5.2			
			34	22	3.0	5.2			
			36	22	3.0	5.2			
			40	22	3.0	5.2			
7b	Pull socket pins to source voltage	40-pin socket	3	20	9.5	10.5			
			6	20	9.5	10.5			
			8	20	9.5	10.5			
			10	20	9.5	10.5			
			12	20	9.5	10.5			
			13	20	9.5	10.5			
			16	20	9.5	10.5			
			19	20	9.5	10.5			
			23	20	9.5	10.5			
			34	20	9.5	10.5			
			35	20	9.5	10.5			
			37	20	9.5	10.5			
			38	20	9.5	10.5			
			39	20	9.5	10.5			

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

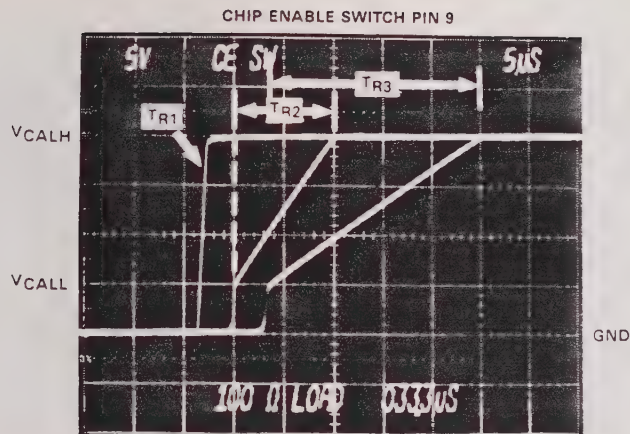
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
7b (cont.)		44-pin socket	1	22	9.5	10.5			
			3	22	9.5	10.5			
			5	22	9.5	10.5			
			7	22	9.5	10.5			
			9	22	9.5	10.5			
			11	22	9.5	10.5			
			15	22	9.5	10.5			
			17	22	9.5	10.5			
			20	22	9.5	10.5			
			22	22	9.0	10.5			
			26	22	9.0	10.5			
			37	22	9.0	10.5			
			38	22	9.0	10.5			
			41	22	9.0	10.5			
			42	22	9.0	10.5			
			43	22	9.0	10.5			
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.)									
8	Backwards device test	40-pin socket	4	20					Connect 10-ohm/5W resistor across pins 4 and 20. Confirm error 32.
(Step numbers 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.)									
9	Low range over-current tests								
9a	VCC	40-pin socket	40	20					Connect 20-ohm/5W resistor across pins 40 and 20. Confirm error 31.
		44-pin socket	1	22					Connect 20-ohm/5W resistor across pins 11 and 22. Confirm error 31.
9b	CE switch	40-pin socket	11	20					Connect 30-ohm/5W resistor across pins 11 and 20. Confirm error 31.
9c	Bit switch 1	40-pin socket	5	20					Connect 30-ohm/5W resistor across pins 5 and 20. Confirm error 20.
9d	Bit switch 2	40-pin socket	1	20					Connect 30-ohm/5W resistor across pins 1 and 20. Confirm error 31.
10	High range tests								

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10a	Normal-current test	40-pin socket	40	20					Connect 20-ohm/5W resistor across pins 40 and 20. Confirm no error.
		40-pin socket	11	20					Connect 30-ohm/5W resistor across the listed pins and confirm no error.
			5	20					
			1	20					
10b	Overcurrent test VCC	40-pin socket	40	20					Connect 5-ohm/5W resistor across pins 40 and 20. Confirm error 31.
10c	Overcurrent test CE switch	40-pin socket	11	20					Connect 12-ohm/5W resistor across pins 11 and 20. Confirm error 31.
10d	Overcurrent test Bit switch 1	40-pin socket	5	20					Connect 12-ohm/5W resistor across pins 5 and 20. Confirm error 31.
10e	Overcurrent test Bit switch 2	40-pin socket	1	20					Connect 12-ohm/5W resistor across pins 1 and 20. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no code has been entered. To enter the family and pinout code; press COPY DEVICE RAM START and enter a family and pinout code, for example - 26/96. Press the START key.									
12	Static programming levels tests								
12a	Family/pinout code 26/96								
	VCC supply - Vccp	40-pin socket	40	20	5.0	5.5	5.25		Enter fuse 32 at the 0000 prompt.
	CE supply - Vihh	40-pin socket	21	20	3.5	5.2			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, programming algorithm								
	Not necessary for calibration - may be used to verify active programming signals.								
14	Optional waveform observation, programming algorithm								
	Not necessary for calibration - may be used to verify active programming signals.								

Table A-9. Calibration Procedure, LogicPak with 303A-010 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
15	This step is not used.								
16	Rise time checks and adjustment								
	CE switch	40-pin socket	11	20	9.0us	11.0us			Adjust R1 on Rise Time Comp. for TR2 as socket shown in figure A-17. Connect 100-ohm, 5%, 2W resistor across pins 11 and 20.
17	Supply linearity test								
	VCC supply	40-pin socket	40	20					Verify waveforms as shown in figure A-18.
	CEsupply	40-pin socket	11	20					Verify waveforms as shown in figure A-18.
	Bit supply	40-pin socket	1	20					The Bit waveforms should be linear as shown in figure A-18.

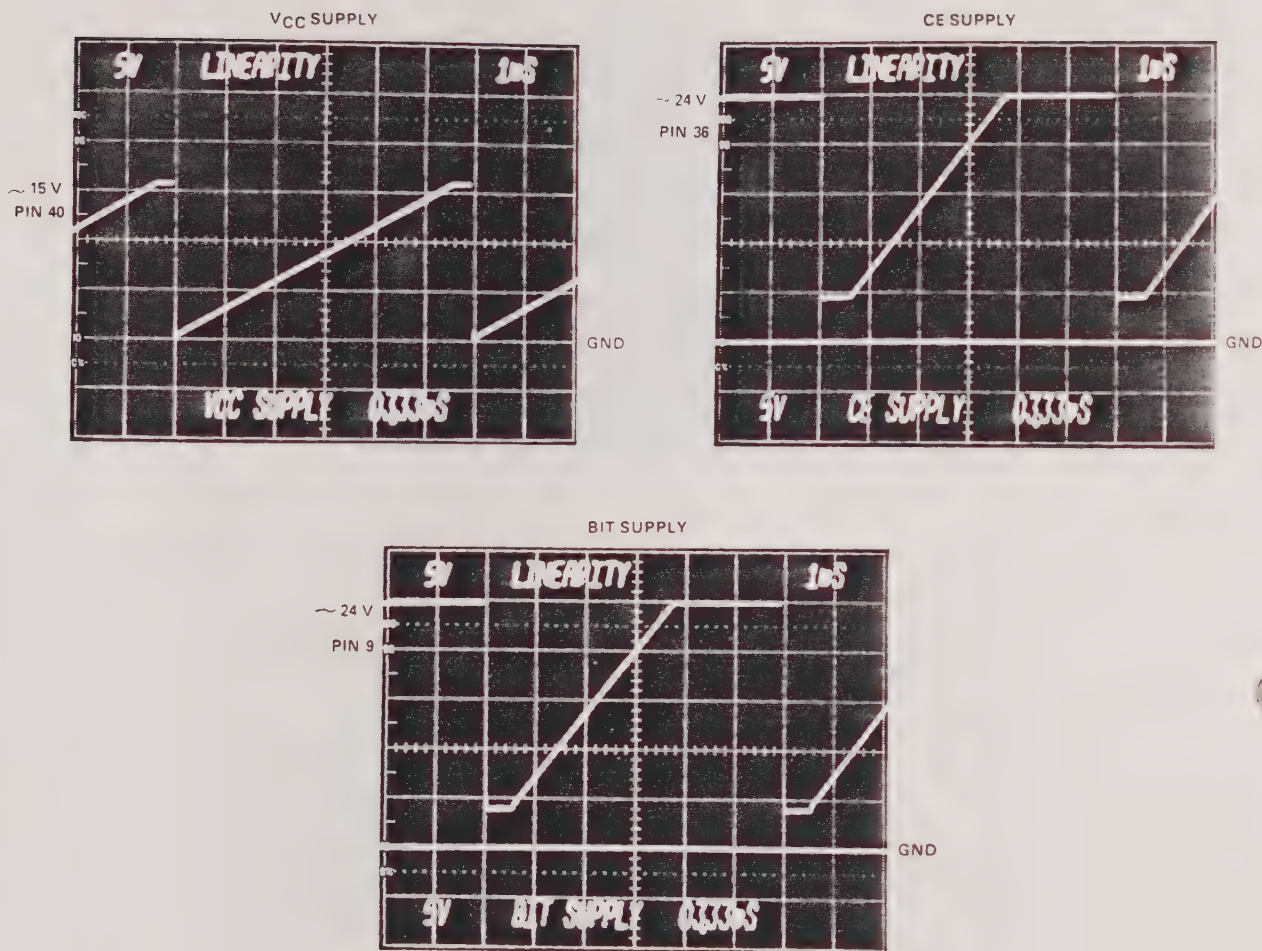


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VcalH	--	20	--	V	Adjust R1 on 1941 card for TR2 CE SW as shown. Verify that others are within limits. Rise times are measured from VcalL to VcalH. (Voltage levels for reference only.)
	VcalL	--	5	--	V	
	TR1 CE SW	.450	650	.850	μs	
	TR2 CE SW	9.0	10.0	11.0	μs	
	TR3 CE SW	15.0	20.0	25.0	μs	

NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 40-pin socket.
3. All waveforms shown loaded by 100 Ω 2W 5% resistor to ground.

Figure A-17. 303A-010 Calibration Waveforms, Step 16



- NOTES
1. Oscilloscope trigger: TP1 on the Waveform Generator Board
 2. Test points are for the 40-pin socket.

Figure A-18. 303A-010 Calibration Waveforms, Step 17

303A-011A P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-011A P/T Adapter, make certain that you are using the 303A-011A Calibration Procedure.

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

IMPORTANT - Prior to starting the calibration procedure, enter the family/pinout code for the socket to be TESTED. To do this, press COPY DEVICE RAM START and enter the family/pinout code for a socket. Use family pinout code 22/44 for the 20 and 24 pin sockets and 01/01 for the 28 pin socket.

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	Pull 20-pin socket pins to TTL low	20-pin socket	1-9 11-20	10-0.4 10	0.8 -0.4	0.8			
	Pull 24-pin socket pins to TTL low	24-pin socket	1-11 13-24	12 12	-0.4 -0.4	0.8 0.8			
	Pull 28-pin socket pins to TTL low	28-pin socket	1-13 15-28	14 14	-0.4 -0.4	0.8 0.8			

CAUTION

Do not leave programmer unattended in calibration mode beyond step 1.

2	Sink drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors the display remains unchanged.
3	Socket LED test								Confirm 20-pin socket LED is off. Confirm 24-pin socket LED is on. Confirm 28-pin socket LED is off.
3a	Comparator reference voltage	Waveform TP5 Generator Board (WGB) and 24-pin socket.	12	10.20	10.28	10.24		R28/WGB	Waveform Generator Board is abbreviated as WGB.

Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3. Remove immediately after performing test or return to test 1.

3b	VCC supply test and adjustment	20-pin socket	20	10	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 20 and 10.
		24-pin socket	24	12	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 24 and 12.
		28-pin socket	28	14	11.9	12.1	12.0	R9/WGB	Connect 50-ohm/5W resistor across pins 28 and 14.

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
3c	CE supply test and adjustment	24-pin socket	13	12	19.8	20.2	20.0	R31/WGB	Connect 100-ohm/5W resistor across pins 13 and 12.
3d	Bit supply switch 1 test and adjustment	24-pin socket	19	12	19.8	20.2	20.0	R6/WGB	Connect 100-ohm/5W resistor across pins 19 and 12.
3e	Bit supply switch 2 test and adjustment	24-pin socket	14	12	19.8	20.2	20.0	NA	Connect 100-ohm/5W resistor across pins 14 and 12.
3f	DAC reference voltage	WGB and 24-pin socket	TP6	12	4.6	5.4			
4	Source drivers test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are E0-FF.
4a	20-pin socket LED test								Confirm that the 20-pin socket LED is on and that the 24-pin and 28-pin socket LEDs are off.
4b	Pull socket pins to TTL high	20-pin socket	2	10	3.0	5.2			
			4	10	3.0	5.2			
			6	10	3.0	5.2			
			8	10	3.0	5.2			
			11	10	3.0	5.2			
			13	10	3.0	5.2			
			15	10	3.0	5.2			
			17	10	3.0	5.2			
			19	10	3.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
		28-pin socket	3	14	3.0	5.2			
			5	14	3.0	5.2			
			7	14	3.0	5.2			
			9	14	3.0	5.2			
			11	14	3.0	5.2			
			13	14	3.0	5.2			
			16	14	3.0	5.2			
			18	14	3.0	5.2			
			21	14	3.0	5.2			
			23	14	3.0	5.2			
			25	14	3.0	5.2			
			27	14	3.0	5.2			

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4c	Pull socket pins to TTL low	20-pin socket	1	10	-0.4	0.8			
			3	10	-0.4	0.8			
			5	10	-0.4	0.8			
			7	10	-0.4	0.8			
			9	10	-0.4	0.8			
			12	10	-0.4	0.8			
			14	10	-0.4	0.8			
			16	10	-0.4	0.8			
			18	10	-0.4	0.8			
		24-pin socket	1	12	-0.4	0.8			
			3	12	-0.4	0.8			
			5	12	-0.4	0.8			
			7	12	-0.4	0.8			
			9	12	-0.4	0.8			
			11	12	-0.4	0.8			
			14	12	-0.4	0.8			
			15	12	-0.4	0.8			
			17	12	-0.4	0.8			
			20	12	-0.4	0.8			
			22	12	-0.4	0.8			
		28-pin socket	1	14	-0.4	0.8			
			2	14	-0.4	0.8			
			4	14	-0.4	0.8			
			6	14	-0.4	0.8			
			8	14	-0.4	0.8			
			10	14	-0.4	0.8			
			12	14	-0.4	0.8			
			15	14	-0.4	0.8			
			17	14	-0.4	0.8			
			19	14	-0.4	0.8			
			20	14	-0.4	0.8			
			22	14	-0.4	0.8			
			24	14	-0.4	0.8			
			26	14	-0.4	0.8			
5	20-pin socket LED test								Confirm that the 28- pin socket LED is on and that the 20-pin and 24-pin socket LEDs are off.
5a	Pull socket pins to TTL low	20-pin socket	2	10	-0.4	0.8			
			4	10	-0.4	0.8			
			6	10	-0.4	0.8			
			8	10	-0.4	0.8			
			11	10	-0.4	0.8			
			13	10	-0.4	0.8			
			15	10	-0.4	0.8			
			17	10	-0.4	0.8			
			19	10	-0.4	0.8			
		24-pin socket	2	12	-0.4	0.8			
			4	12	-0.4	0.8			
			6	12	-0.4	0.8			
			8	12	-0.4	0.8			
			10	12	-0.4	0.8			
			13	12	-0.4	0.8			
			16	12	-0.4	0.8			
			18	12	-0.4	0.8			
			19	12	-0.4	0.8			
			21	12	-0.4	0.8			
			23	12	-0.4	0.8			

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)		Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.	
5a (cont.)		28-pin socket	3	14	-0.4	0.8		
			5	14	-0.4	0.8		
			7	14	-0.4	0.8		
			9	14	-0.4	0.8		
			11	14	-0.4	0.8		
			13	14	-0.4	0.8		
			16	14	-0.4	0.8		
			18	14	-0.4	0.8		
			21	14	-0.4	0.8		
			23	14	-0.4	0.8		
			25	14	-0.4	0.8		
			27	14	-0.4	0.8		
5b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2		
			3	10	3.0	5.2		
			5	10	3.0	5.2		
			7	10	3.0	5.2		
			9	10	3.0	5.2		
			12	10	3.0	5.2		
			14	10	3.0	5.2		
			16	10	3.0	5.2		
			18	10	3.0	5.2		
		24-pin socket	1	12	3.0	5.2		
			3	12	3.0	5.2		
			5	12	3.0	5.2		
			7	12	3.0	5.2		
			9	12	3.0	5.2		
			11	12	3.0	5.2		
			14	12	3.0	5.2		
			15	12	3.0	5.2		
			17	12	3.0	5.2		
			20	12	3.0	5.2		
			22	12	3.0	5.2		
		28-pin socket	1	14	3.0	5.2		
			2	14	3.0	5.2		
			4	14	3.0	5.2		
			6	14	3.0	5.2		
			8	14	3.0	5.2		
			10	14	3.0	5.2		
			12	14	3.0	5.2		
			15	14	3.0	5.2		
			17	14	3.0	5.2		
			19	14	3.0	5.2		
			20	14	3.0	5.2		
			22	14	3.0	5.2		
			24	14	3.0	5.2		
			26	14	3.0	5.2		
6a	Pull socket pins to source voltage	20-pin socket	2	10	9.0	10.5		
			4	10	9.0	10.5		
			6	10	9.0	10.5		
			8	10	9.0	10.5		
			11	10	9.0	10.5		
			13	10	9.0	10.5		
			15	10	9.0	10.5		
			17	10	9.0	10.5		
			19	10	9.0	10.5		

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
6a (cont.)	24-pin socket		2	12	9.0	10.5			
			4	12	9.0	10.5			
			6	12	9.0	10.5			
			8	12	9.0	10.5			
			10	12	9.0	10.5			
			13	12	9.0	10.5			
			14	12	9.0	10.5			
			16	12	9.0	10.5			
			18	12	9.0	10.5			
			19	12	9.0	10.5			
			21	12	9.0	10.5			
			23	12	9.0	10.5			
	28-pin socket		1	14	9.0	10.5			
			3	14	9.0	10.5			
			5	14	9.0	10.5			
			7	14	9.0	10.5			
			9	14	9.0	10.5			
			11	14	9.0	10.5			
			13	14	9.0	10.5			
			16	14	9.0	10.5			
			18	14	9.0	10.5			
			21	14	9.0	10.5			
			23	14	9.0	10.5			
			25	14	9.0	10.5			
			27	14	9.0	10.5			
6b	Pull socket pins to TTL high	20-pin socket	1	10	3.0	5.2			
			3	10	3.0	5.2			
			5	10	3.0	5.2			
			7	10	3.0	5.2			
			9	10	3.0	5.2			
			12	10	3.0	5.2			
			14	10	3.0	5.2			
			16	10	3.0	5.2			
			18	10	3.0	5.2			
		24-pin socket	1	12	3.0	5.2			
			3	12	3.0	5.2			
			5	12	3.0	5.2			
			7	12	3.0	5.2			
			9	12	3.0	5.2			
			11	12	3.0	5.2			
			15	12	3.0	5.2			
			17	12	3.0	5.2			
			20	12	3.0	5.2			
			22	12	3.0	5.2			
		28-pin socket	2	14	3.0	5.2			
			4	14	3.0	5.2			
			6	14	3.0	5.2			
			8	14	3.0	5.2			
			10	14	3.0	5.2			
			12	14	3.0	5.2			
			15	14	3.0	5.2			
			17	14	3.0	5.2			
			19	14	3.0	5.2			
			20	14	3.0	5.2			
			22	14	3.0	5.2			
			24	14	3.0	5.2			
			26	14	3.0	5.2			

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
7a	Pull socket pins to TTL high	20-pin socket	2	10	1.0	5.2			
			4	10	1.0	5.2			
			6	10	1.0	5.2			
			8	10	1.0	5.2			
			11	10	1.0	5.2			
			13	10	1.0	5.2			
			15	10	1.0	5.2			
			17	10	1.0	5.2			
			19	10	1.0	5.2			
		24-pin socket	2	12	3.0	5.2			
			4	12	3.0	5.2			
			6	12	3.0	5.2			
			8	12	3.0	5.2			
			10	12	3.0	5.2			
			13	12	3.0	5.2			
			14	12	3.0	5.2			
			16	12	3.0	5.2			
			18	12	3.0	5.2			
			19	12	3.0	5.2			
			21	12	3.0	5.2			
			23	12	3.0	5.2			
		28-pin socket	1	14	3.0	5.2			
			3	14	3.0	5.2			
			5	14	3.0	5.2			
			7	14	3.0	5.2			
			9	14	3.0	5.2			
			11	14	3.0	5.2			
			13	14	3.0	5.2			
			16	14	3.0	5.2			
			18	14	3.0	5.2			
			21	14	3.0	5.2			
			23	14	3.0	5.2			
			25	14	3.0	5.2			
			27	14	3.0	5.2			
7b	Pull socket pins to source voltage	20-pin socket	1	10	9.0	10.5			
			3	10	9.0	10.5			
			5	10	9.0	10.5			
			7	10	9.0	10.5			
			9	10	9.0	10.5			
			12	10	9.0	10.5			
			14	10	9.0	10.5			
			16	10	9.0	10.5			
			18	10	9.0	10.5			
		24-pin socket	1	12	9.0	10.5			
			3	12	9.0	10.5			
			5	12	9.0	10.5			
			7	12	9.0	10.5			
			9	12	9.0	10.5			
			11	12	9.0	10.5			
			15	12	9.0	10.5			
			17	12	9.0	10.5			
			20	12	9.0	10.5			
			22	12	9.0	10.5			

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

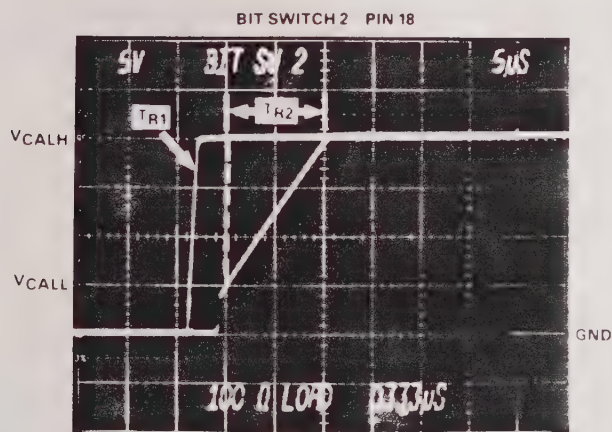
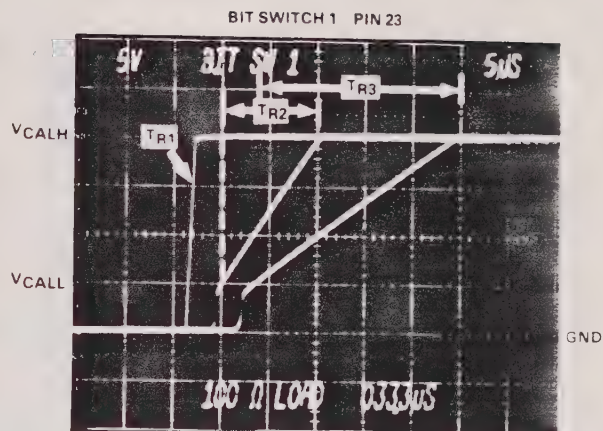
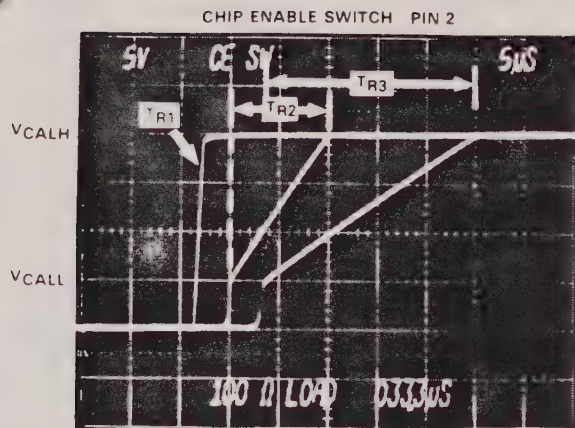
Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
7b (cont.)		28-pin socket	2	14	9.0	10.5			
			4	14	9.0	10.5			
			6	14	9.0	10.5			
			8	14	9.0	10.5			
			10	14	9.0	10.5			
			12	14	9.0	10.5			
			15	14	9.0	10.5			
			17	14	9.0	10.5			
			19	14	9.0	10.5			
			20	14	9.0	10.5			
			22	14	9.0	10.5			
			24	14	9.0	10.5			
			26	14	9.0	10.5			
Before performing steps 8 and 9, insert the appropriate load resistor (after pressing START to advance to step 8). Remove immediately after performing test or return to test 1.									
8	Backwards device test	28-pin socket	28	14					Connect 10-ohm/5W resistor across pins 28 and 14. Confirm error 31.
Steps 9 through 17 cannot be accessed by pressing the START key. Once you have performed tests 1-8, the programmer will not advance to the other calibration steps, or review previous steps. To continue calibration with step 9, press SELECT C1 START 9 START. Use this key sequence, substituting the calibration step you want to perform for the example step 9 to select each calibration step.									
9	Low range over-current tests								
9a	VCC	28-pin socket	28	14					Connect 20-ohm/5W resistor across pins 28 and 14. Confirm error 31.
9b	CE switch	28-pin socket	5	14					Connect 30-ohm/5W resistor across pins 5 and 14. Confirm error 31.
9c	Bit switch 1	28-pin socket	13	14					Connect 30-ohm/5W resistor across pins 13 and 14. Confirm error 31.
9d	Bit switch 2	28-pin socket	1	14					Connect 30-ohm/5W resistor across pins 1 and 14. Confirm error 31.
10	High range over-current tests								
10a	VCC	28-pin socket	28	14					Connect 5-ohm/5W resistor across pins 28 and 14. Confirm error 31.

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
10b	CE switch	28-pin socket	5	14					Connect 12-ohm/5W resistor across pins 5 and 14. Confirm error 31.
10c	Bit switch 1	28-pin socket	13	14					Connect 12-ohm/5W resistor across pins 13 and 14. Confirm error 31.
10d	Bit switch 2	28-pin socket	1	14					Connect 12-ohm/5W resistor across pins 1 and 14. Confirm error 31.
11	Skip this step; not used for calibration								
Before continuing with the calibration steps 12, 13, and 14, you must enter the family and pinout code. Error 30 will occur if no device code has been entered. To enter the family and pinout code; Press COPY DEVICE RAM and enter a family and pinout code, for example - 9804. Press the START key. 22/17									
12	Static programming levels tests								
12a	Family code 22/17								Enter family code 22/17. Enter fuse 32 at the 0000 prompt.
	VCC supply - Vccp	20-pin socket	20	10	11.5	12.0			
	CE supply - Vihh	20-pin socket	1	10	11.5	12.0			
	Bit supply - Vihh	20-pin socket	19	10	11.5	12.0			
12b	Family code 30/17								Enter family code 30/17. Enter fuse 32 at the 0000 prompt.
	VCC supply - Vccp	20-pin socket	20	10	9.75	10.25			
	CE supply - Vihh	20-pin socket	1	10	9.75	10.25			
	Bit supply - Vihh	20-pin socket	19	10	9.75	10.2			
The waveforms for steps 13 and 14 are available upon request. Contact your Data I/O service representative.									
13	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals
14	Optional waveform observation, programming algorithm								Not necessary for calibration - may be used to verify active programming signals.

Table A-10. Calibration Procedure, LogicPak with 303A-011A P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
15	This step is not used.								
16	Rise time checks and adjustment								
	CE switch	24-pin socket	2	12	9.0us	11.0us			Adjust R1 on Rise Time Comp. for TR2 as shown on waveforms in figure A-19. Connect 100-ohm, 5% 2W resistor across pins 2 and 12.
	Bit switch 1	24-pin socket	23	12	8.0us	12.0us			Connect 100-ohm/5% 2W resistor across pins 23 and 12.
	Bit switch 2	24-pin socket	18	12	8.0us	12.0us			Connect 100-ohm/5% 2W resistor across pins 18 and 12.
17	Supply linearity test								
	VCC supply	24-pin socket	24	12					Verify waveforms as shown in figure A-20.
	CE supply	24-pin socket	6	12					Verify waveforms as shown in figure A-20.
	Bit supply	24-pin socket	19	12					The Bit waveforms should be linear as shown in figure A-20.

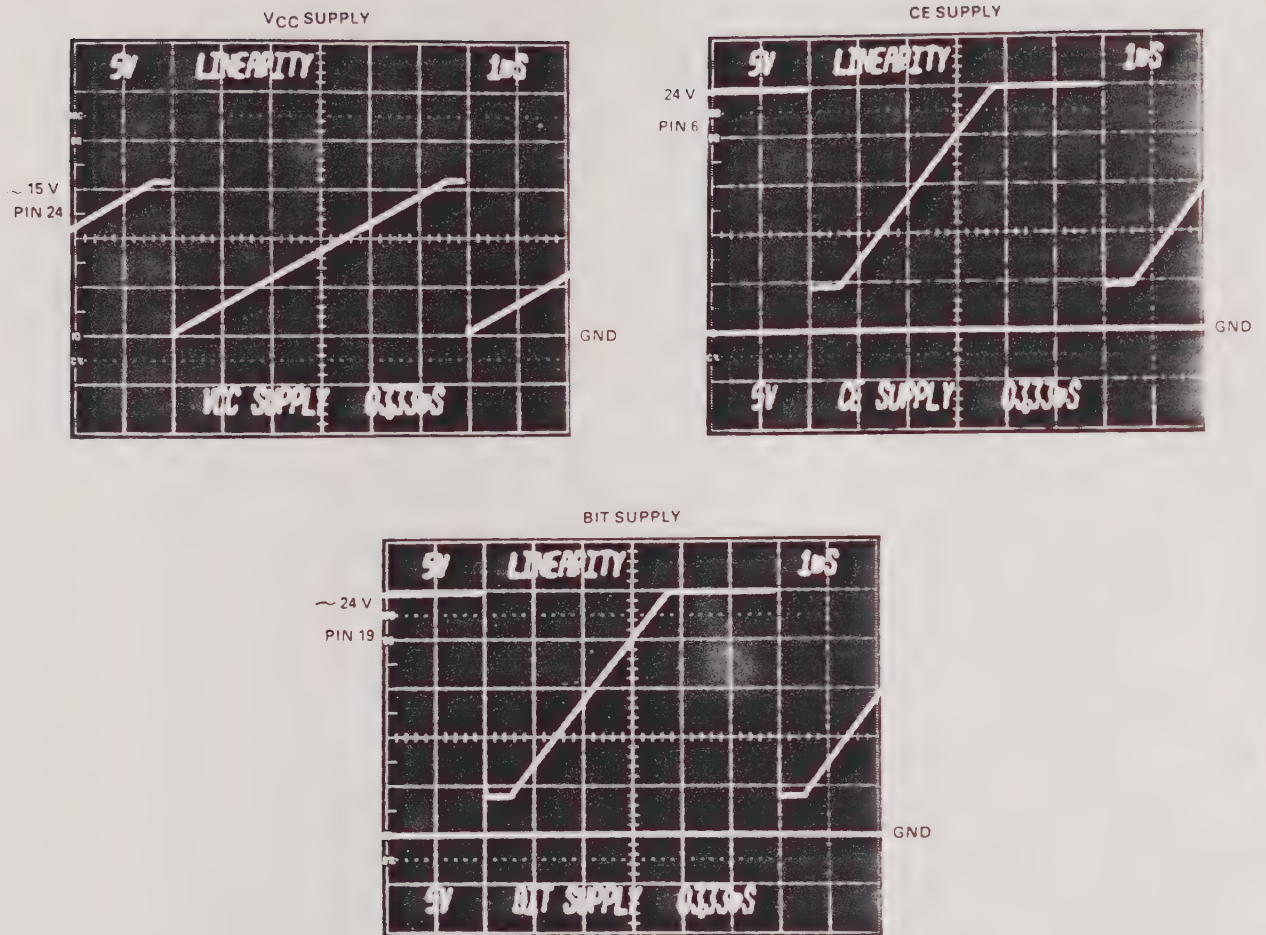


	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V _{CALLH}		20		V	
	V _{CALL}		5		V	
	T _{R1} CE SW	450	650	850	μ S	Adjust R1 on 1941 card for T _{R2} CE SW as shown. Verify that others are within limits. Rise times are measured from V _{CALL} to V _{CALLH} . (Voltage levels for reference only)
	T _{R2} CE SW	9.0	10.0	11.0	μ S	
	T _{R3} CE SW	15.0	20.0	25.0	μ S	
	T _{R1} BIT SW	450	650	850	μ S	
	T _{R2} BIT SW	8.0	10.0	12.0	μ S	
	T _{R3} BIT SW	15.0	20.0	25.0	μ S	

NOTES

- Oscilloscope trigger: TP1 on the Waveform Generator Board
- Test points are for the 24-pin socket
- BIT SW rise time limits are for both BIT SW1 and BIT SW2
- All waveforms shown loaded by 100 Ω 2W 5% resistor to ground

Figure A-19. 303A-011A Calibration Waveforms, Step 16



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board
2. Test points are for the 24-pin socket

Figure A-20. 303A-011A Calibration Waveforms, Step17

303A-011B P/T ADAPTER CALIBRATION PROCEDURE

There is no Calibration Test Procedure for the 303A-011B P/T Adapter due to the sensitivity of the adapter sockets and the high risk of possible damage. Contact your local Data I/O Customer Support Representative if any problems arise. Included, however, is the Acceptance Test Procedure for the LogicPak and P/T Adapters that will check for correct current/voltages to the socket pins and verify proper operation.

303A-012 P/T ADAPTER CALIBRATION PROCEDURE

CAUTION

Before calibrating your LogicPak using the 303A-012 P/T Adapter, make certain that you are using the 303A-012 Calibration Procedure.

Table A-11. Calibration Procedure, LogicPak with 303A-012 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
1	All pins low	28-pin socket/ all pins. 20-pin socket/ all pins 24 pin socket/ all pins			-0.4	0.8	0.0		Ground DVM to pin 10 of 20-pin, pin 12 of 24-pin, or pin 14 of 28-pin socket.
CAUTION									
Do not leave programmer unattended in calibration mode beyond step 1.									
2	Sink drivers test, self test								See Table 5-3 if errors result. Errors must be corrected to continue. Possible errors are A0-DF. If there are no errors, the display remains unchanged.
3a	Socket LED test 1								Confirm 28-pin socket LED is on; others are off.
Before performing steps 3b through 3e, insert the appropriate load resistor (after pressing the START key to advance to step 3. Remove immediately after performing test or return to test 1.)									
3b	Comparator reference	TP5/ 701-1935			10.28	10.24		R28 701-1939	
3c	VCC supply test	28-pin socket/ pin 28			11.9	12.1	12.0	R9 701-1939	Connect 50-ohm/5W resistor to ground.
3d	CE supply test and adjustment	28-pin socket/ pin 5			19.8	20.2	20.0	R31 701-1939	Connect 100-ohm/5W resistor to ground.
3e	Bit supply switch 1	28-pin socket/ socket, pin 15			19.8	20.2	20.0	R6 701-1939	Connect 100-ohm/5W resistor to ground.
3f	Bit supply switch 2	24-pin socket, pin 14			19.0	20.0	19.4		Connect 100-ohm/5W resistor to ground.
3g	DAC reference voltage	701-1939/TP6			4.7	5.3	5.0		
4a	LED test								Confirm that the 24- pin socket LED is on; all others are off.
4b	Self test voltage/ current sources								If errors result, - see error codes table.
4c	Socket pins TTL high	28-pin socket/ pins 3,5,7,9,10 12,15,19,21,23,25,27. 24-pin socket/ pins 13 and 16.			3.0	5.2	5.0		

Table A-11. Calibration Procedure, LogicPak with 303A-012 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
4d	Socket pins TTL low	28-pin socket/ pins 2,4,6,8,11,13, 16,18,20,22,24,26. 24-pin socket/ pins 15 and 17.			-0.4	0.8	0		
5a	Socket pins TTL low	28-pin socket/ pins 3,5,7,9,10,12,15, 19,21,23,25,27. 24-pin socket/ pins 13 and 16.			-0.4	0.8	0		
5b	Socket pins TTL high	28-pin socket/ pins 2,4,6,8,11,13, 16,18,20,22,24,26. 24-pin socket/ pins 15 and 17.			3.0	5.2	5.0		
5c	LED test 3								Confirm 20-pin LED on; all others off.
6a	Socket pins source	28-pin socket/ pins 3,5,7,9,10,12,15, 19,21,23,25,27. 24-pin socket/ pins 14 and 16.			9.0	10.5	9.75		
6b	Socket pins TTL high	28-pin socket/ pins 2,4,6,8,11,13, 16,18,20,22,24,26. 24-pin socket/ pins 15 and 17.			3.0	5.2	5.5		
7a	Socket pins TTL high	28-pin socket/ pins 3,5,7,9,10,12,15, 19,21,23,25,27. 24-pin socket/ pins 14 and 16.			3.0	5.2	5		
7b	Socket pins source	28-pin socket/ pins 2,4,6,8,11,13, 16,18,20,22,24,26. 24-pin socket/ pins 15 and 17.			9.0	10.5	9.75		
8	Backwards device test	28-pin socket/ pin 28							Load with 10-ohm resistor to ground; verify that error 32 is generated.
9a	Low-range test	28-pin socket/ pin 28							Load with 5W, 20-ohm resistor to ground; verify that error 31 is generated.
9b	CE switch test	28-pin socket/ pin 5							Load with 5W, 30-ohm resistor to ground; verify that error 31 is generated.

Table A-11. Calibration Procedure, LogicPak with 303A-012 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
9c	Bit switch 1 test	28-pin socket/ pin 10							Load with 5W, 30-ohm resistor to ground; verify that error 31 is generated.
9d	Bit switch 2 test	28-pin socket/ pin 19							Load with 5W, 30-ohm resistor to ground; verify that error 31 is generated.
10a	High range overcurrent test	28-pin socket/ pin 28							Load with 5W, 5-ohm resistor to ground; verify that error 31 is generated.
10b	CE switch	28-pin socket/ pin 5							Load with 12W, 5-ohm resistor to ground; verify that error 31 is generated.

NOTE

Family pinout code 1A 33 must now be keyed in; otherwise, the error message "PROGRAM PAK ERROR 30" will appear on the programmer's display.

10c	Bit switch 1	28-pin socket/ pin 10							Load with 12W, 5-ohm resistor to ground; verify that error 31 is generated.
10d	Bit switch 2	28-pin socket/ pin 19							Load with 12W, 5-ohm resistor to ground; verify that error 31 is generated.
11	Program last fuse	20-pin socket/ pin 19							Load with 5W, 10-ohm resistor to ground; verify that waveform shown in photo, figure A-21, is generated.
12a	Static program level	28-pin socket/ pin 28			8.5	9.0	8.75		Press SELECT C1 START 10 START, to select fuse #10.
12b	CE switch	28-pin socket/ pin 5			4.75	5.25	5.0		
12c	Bit switch 1	28-pin socket/ pin 12			4.75	5.25	5.0		

Table A-11. Calibration Procedure, LogicPak with 303A-012 P/T Adapter

Step	Test Name	Test Connections (DMM or Scope)			Measurement Limits (volts unless noted)			Adjustment Location	Comments
		Location	High	Low	Min.	Max.	Nom.		
13	Read fuse waveforms								No test for this cal step.
14a	Program fuse waveforms	20-pin socket/ pin 18			.50V/us	1.0V/us	.75V/us	R8/ 701-2105	Load with 5W, 10-ohm resistor to ground; verify that waveform shown in photo, figure A-22, is generated. Adjust R8 on 701-2105 for .75V/us rise rate.
14b	Program fuse waveform	20-pin socket/ pin 1							Change family/pinout code 07 30. Load with 5W, 10-ohm resistor to ground; connect 20-pin socket/ pin 12 directly to ground also. Verify that waveform shown in photo, figure A-23, is generated.
15	Program all fuses from RAM								No test for this cal step.
16a	Rise Time Adjust	28-pin socket/ pin 27			9us	11us	10us	R1/ 701-1941	Adjust for TR2, as shown in photo, figure A-24.
16b	Bit switch 1	28-pin socket/ pin 18			8us	12us			Verify waveform per photo, figure A-25.
16c	Bit switch 2	28-pin socket/ pin 19			8us	12us			Verify waveform per photo, figure A-26.
17a	Supply linearity	28-pin socket/ pin 28							Verify waveform per photo, figure A-27.
17b	CE switch	28-pin socket/ pin 5							Waveforms should be linear as shown, figure A-27.
17c	Bit Switch 1	28-pin socket/ pin 18							0-15V for Vcc, 0-24V for CE, 0-24V for Bit 1.
*18	C3 clock	20-pin socket/ pin 1				16ns			Load with 120-ohm resistor to ground and verify rise time.
*19	Clamp DAC linearity	20-pin socket/ pin 1							Verify waveform per photo, figure A-28. Waveform should be linear between 7-19 volts.

*These steps are not applicable on V01 adapters.

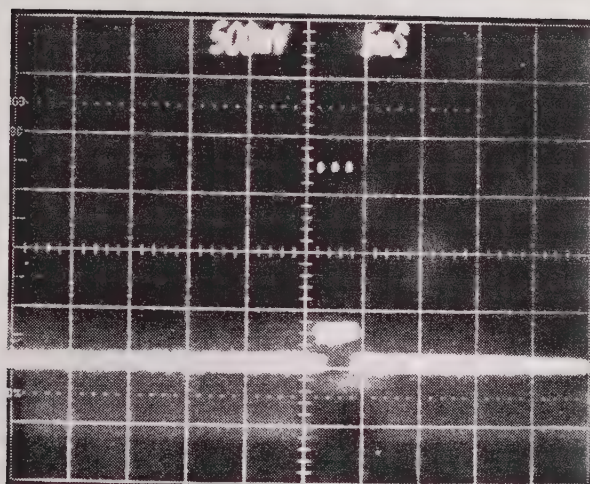


Figure A-21. 303A-012 Calibration Waveform, Step 11

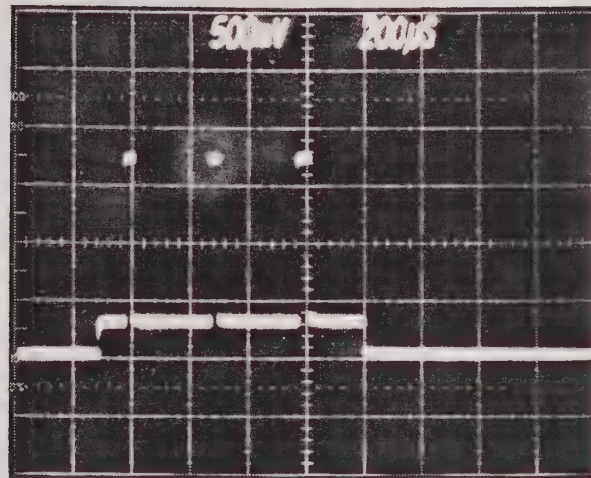


Figure A-22. 303A-012 Calibration Waveform, Step 14a

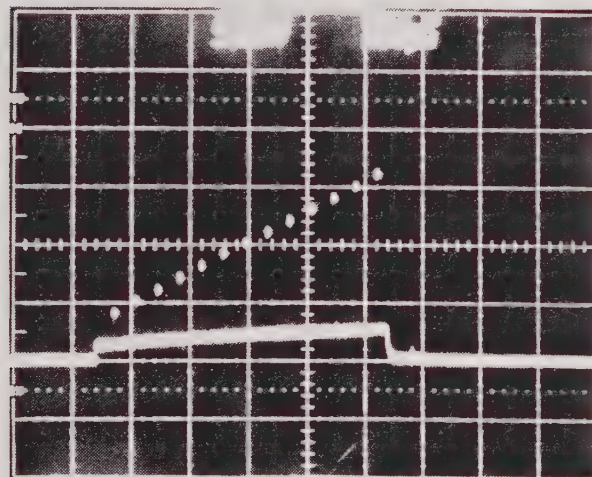


Figure A-23. 303A-012 Calibration Waveform, Step 14b

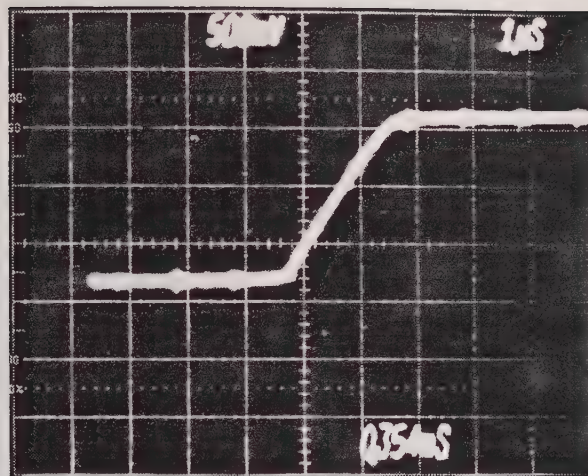


Figure A-24. 303A-012 Calibration Waveform, Step 16a

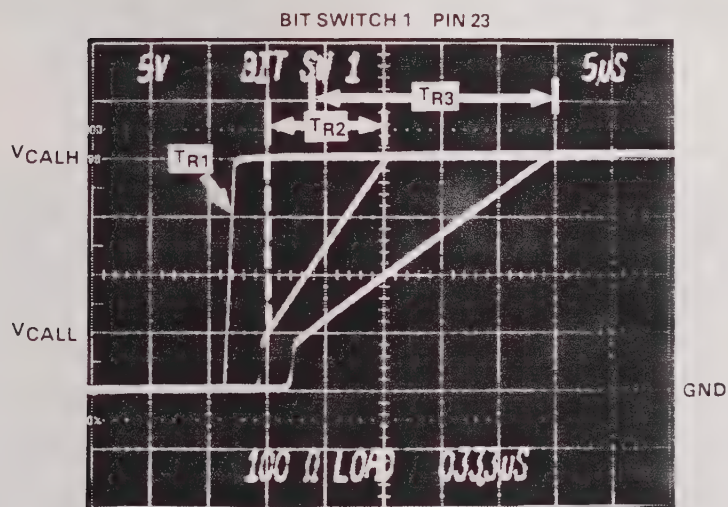


Figure A-25. 303A-012 Calibration Waveform, Step 16b

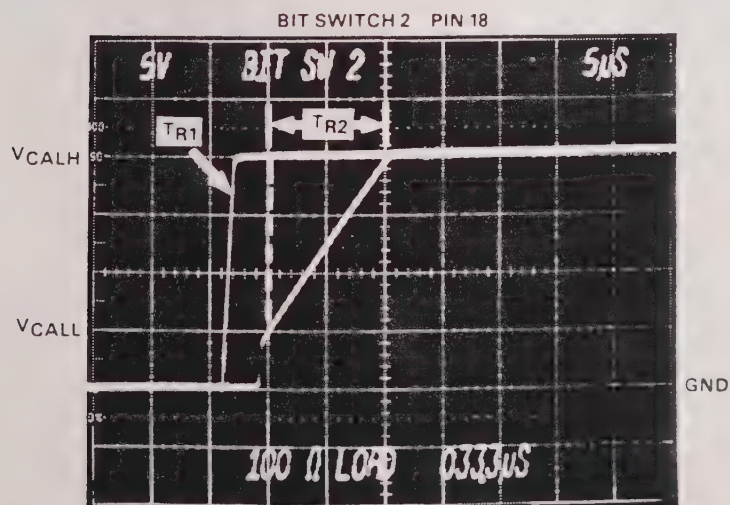
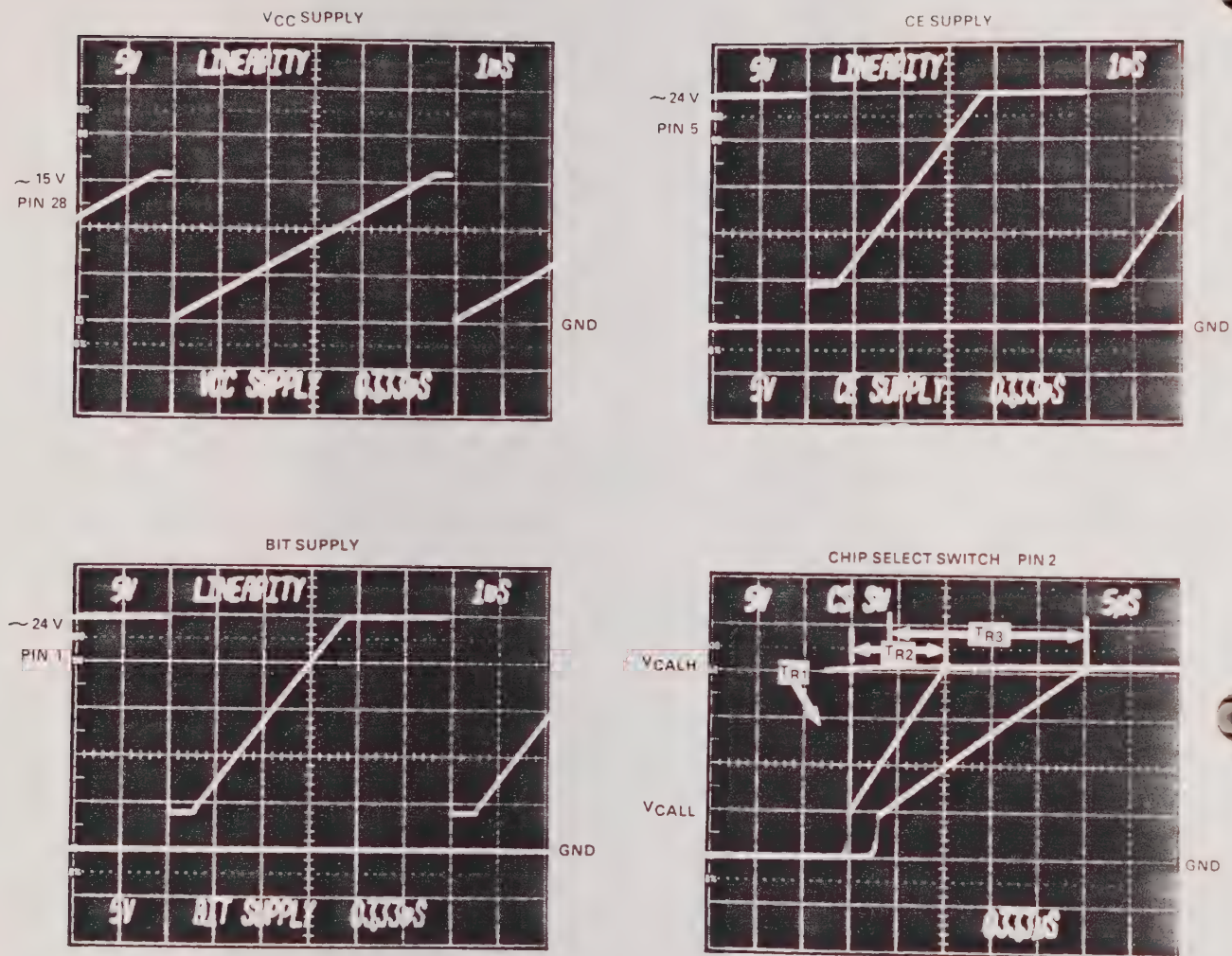


Figure A-26. 303A-012 Calibration Waveform, Step 16c



NOTES

1. Oscilloscope trigger: TP1 on the Waveform Generator Board.
2. Test points are for the 28-pin socket

Figure A-27. 303A-012 Calibration Waveform, Step 17

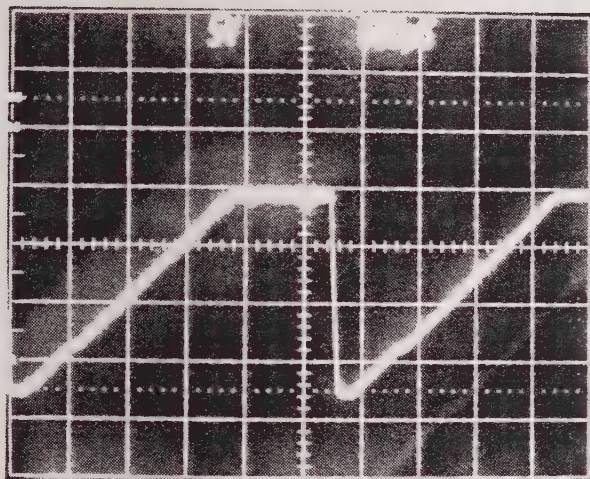


Figure A-28. 303A-012 Calibration Waveform, Step19

ACCEPTANCE TEST PROCEDURE

LogicPak and P/T Adapters

AUGUST 1987

Data I/O Corporation warrants to the original purchaser of the product described by this manual that the product was fully functional to the extent of its specification at the time of shipment from the factory. Data I/O further certifies that the equipment used to test the product was calibrated to standards that are traceable to the national bureau of standards as appropriate. Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment which it accompanies.

This acceptance test procedure is for use with the LogicPak and the following P/T adapters:

303A-001	IFL P/T Adapter
303A-007	Harris CMOS P/T Adapter
303A-008A	32R16 P/T Adapter (DIP + LCC)
303A-008B	32R16 P/T Adapter (DIP + NLCC)
303A-010	Altera/Intel 40-pin P/T Adapter
303A-011A	DIP PLD P/T Adapter
303A-011B	PLCC PLD P/T Adapter
303A-012	AIM P/T Adapter

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LogicPak™ is a trademark of Data I/O Corporation.
IFL™ is a trademark of Signetics Corporation.

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Introduction

This procedure is provided for customers whose company policy requires that a receiving inspection test be performed before the unit may be accepted.

Your LogicPak and/or P/T adapter was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O. Call (800) 247-5700 for the number of your local Service Representative.

The LogicPak performance check consists of a brief self-check procedure to check supply current/voltages to the socket pins to verify proper operation.

Before beginning this test procedure, you must have the following equipment:

- LogicPak
- P/T adapter (see compatibility table)
- Data I/O Programmer (see compatibility table)

The following compatibility table lists the programmers and the minimum RAM required for each P/T adapter.

COMPATIBILITY TABLE

P/T Adapter	Programmer	Minimum Programmer RAM
303A-001	29A, 29B, System 19, Model 100A	8K
303A-007	29A, 29B, System 19, Model 100A	8K
303A-008A/B	29A, 29B	64K
303A-010	29A, 29B	64K
303A-011A	29A, 29B, System 19	16K
303A-011B	29A, 29B, System 19	16K
303A-012	29A, 29B, System 19	16K

Check for additional programmer compatibility requirements in the LogicPak Operator's manual and your P/T adapter User Note.

Table 1-1. Test Procedure. LogicPak 303A with *Any P/T Adapter

For proper hook-up and connections refer to either the LogicPak Operator's manual, the P/T adapter User Notes or your programmer manual.

Step	Test Name	Programmer Key Selection/ Procedure	Programmer Display	Test Performed/ Comments
NA	Power up test	Turn the power switch ON and confirm that no errors are displayed on the front panel.	If any errors occur, contact your local Data I/O Customer Support Center.	When the system is powered up, an internal self-test is performed. This test assures that the firmware in the LogicPak is functioning correctly and that the various voltage supplies are also functioning correctly.

The following procedure steps the equipment through a series of self-tests that assures the equipment is functioning properly. No readings or measurements are required. If any errors occur, note the error number and the step in which it occurred. (The possible errors for a given step are shown in the last column of the procedure.)

NA	NA	SELECT C 1	SELECT CODE ^ SELECT CODE ^ C 1	Selects the calibration mode.
1	All pins go to 0 volts	START START	CAL STEP ^ 01 CAL STEP ^ 01	Checks supply and current voltages.
2	TTL driver self-check	START	CAL STEP ^ 02	TTL driver self-check. Possible errors are 9F-DF.
3	Calibration levels	START	CAL STEP ^ 03	Levels for calibration.
4	Source driver self-check	START	CAL STEP ^ 04	Source driver self-check. Possible errors are E0-FF.

*Check that you are using one of the programmers listed in the Compatibility Table for your P/T adapter.

NOTE

If any errors do occur, note the calibration step number in which the error was detected, the error code displayed, and then contact your local Data I/O Customer Support Center or refer to the calibration procedure for the specific P/T adapter in Appendix B of the LogicPak Maintenance manual.

If your acceptance requirements dictate a full calibration of the unit, contact Data I/O for the maintenance manual for the product.

The preceding procedure, if performed with no errors, provides an adequate functional test of a new LogicPak and/or P/T adapter. Should programming yields become unacceptable, calibration of the unit may be required. If calibration is required, contact your nearest Data I/O Customer Support Center.

APPENDIX B

SCHEMATIC DIAGRAMS

LogicPak

30-702-1938	LogicPak Motherboard, 1 page
30-701-1939	LogicPak Waveform Generator Board, 1 page
30-701-1940	LogicPak Sink Driver Board (old), 1 page
30-701-0131	LogicPak Sink Driver Board (new), 1 page
30-702-1943	LogicPak Pin Driver Board (old), 2 pages
30-701-0143	LogicPak Pin Driver Board (new), 2 pages
30-701-1941	LogicPak Time/Rise Comparator Board, 2 pages
30-701-1942	LogicPak Controller/Memory Board, 2 pages
30-701-1944	LogicPak Extender Board, 1 page

P/T Adapters

30-701-0127	303A-001 PCB, 1 page
30-701-0130	303A-002 PCB, 1 page
30-702-1947	303A-003 PCB and 303A-004 PCB, 1 page
30-701-0046	303A-006 PCB, 2 pages
30-701-0138	303A-007 PCB, 2 pages
30-701-0149	303A-008 Motherboard, 1 page
30-701-0148	303A-008 Intermediate Board, 1 page
30-701-0009	303A-008 Socket Board, 1 page
30-701-0152	303A-009 Component Board, 1 page
30-701-0155	303A-009 Daughter Board, 1 page
30-701-2048	303A-010 Daughter Board, 1 page
30-701-2049	303A-010 Daughter Board, 1 page
30-701-2090	303A-011A/B Motherboard, 1 page
30-701-2091	303A-011A Daughter Board (old), 1 page
30-701-2138	303A-011A Daughter Board (new), 1 page
30-701-2092	303A-011B Daughter Board, 1 page
30-701-2105	303A-012 Motherboard, 1 page
30-701-2104	303A-012 Socket Board, 1 page

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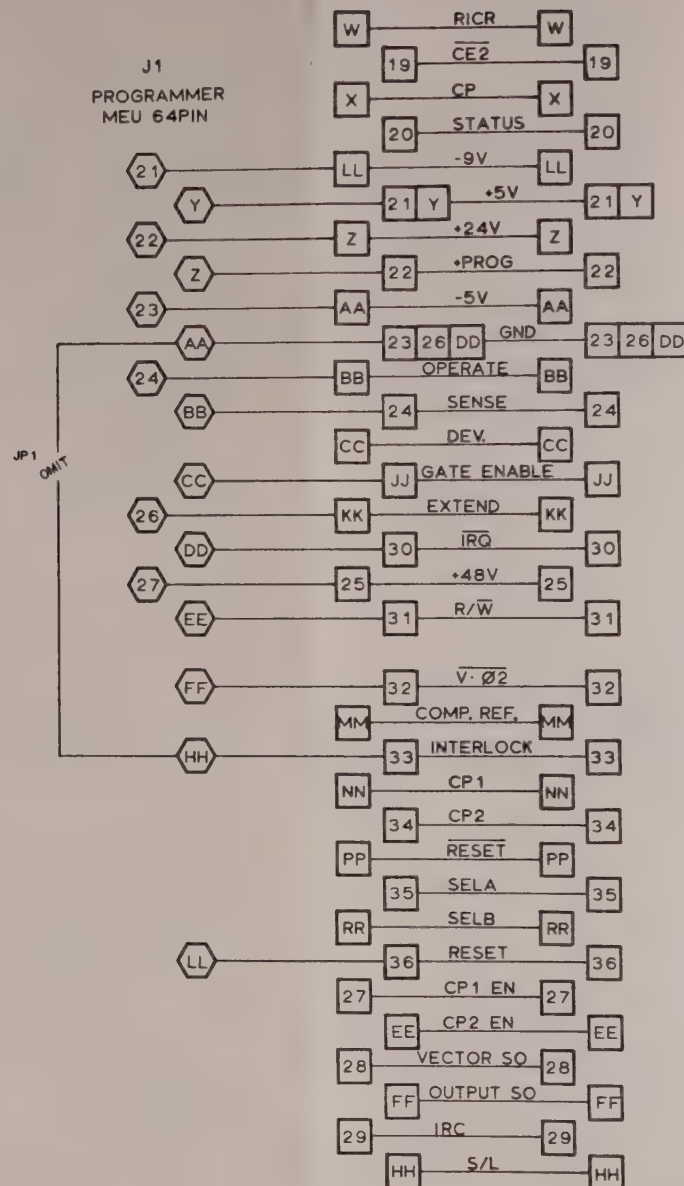
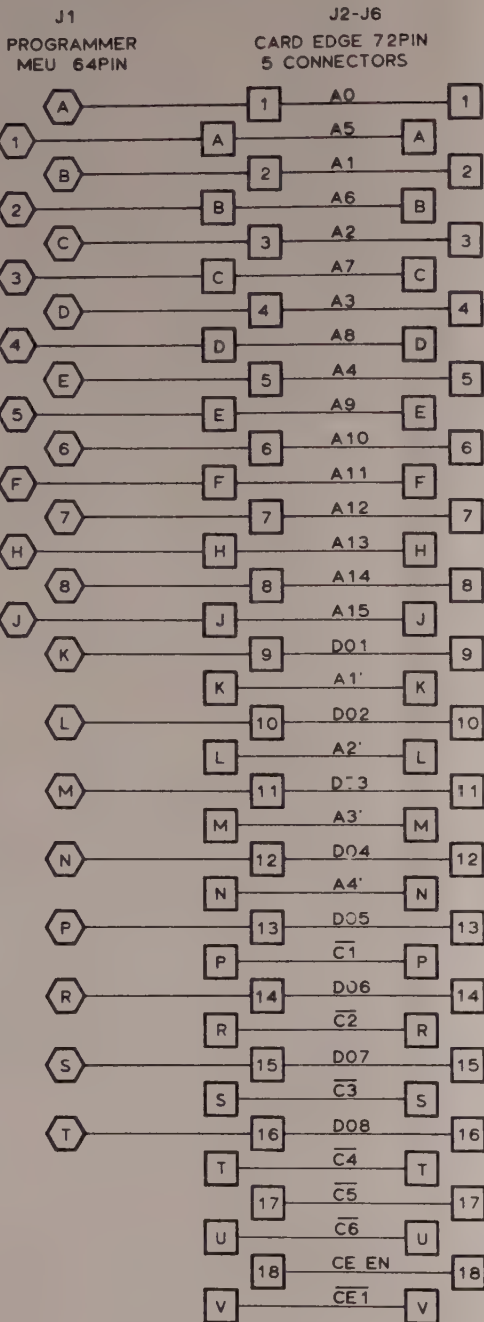
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REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D
A	RELEASE	JK	CS	7/1/82
B	ECN 4891	CL	CS	7/1/82
C	ECN 4785	3/83	SH	1/1/83
D	REFERENCE CMA 0103	BV	CS	1/4/86

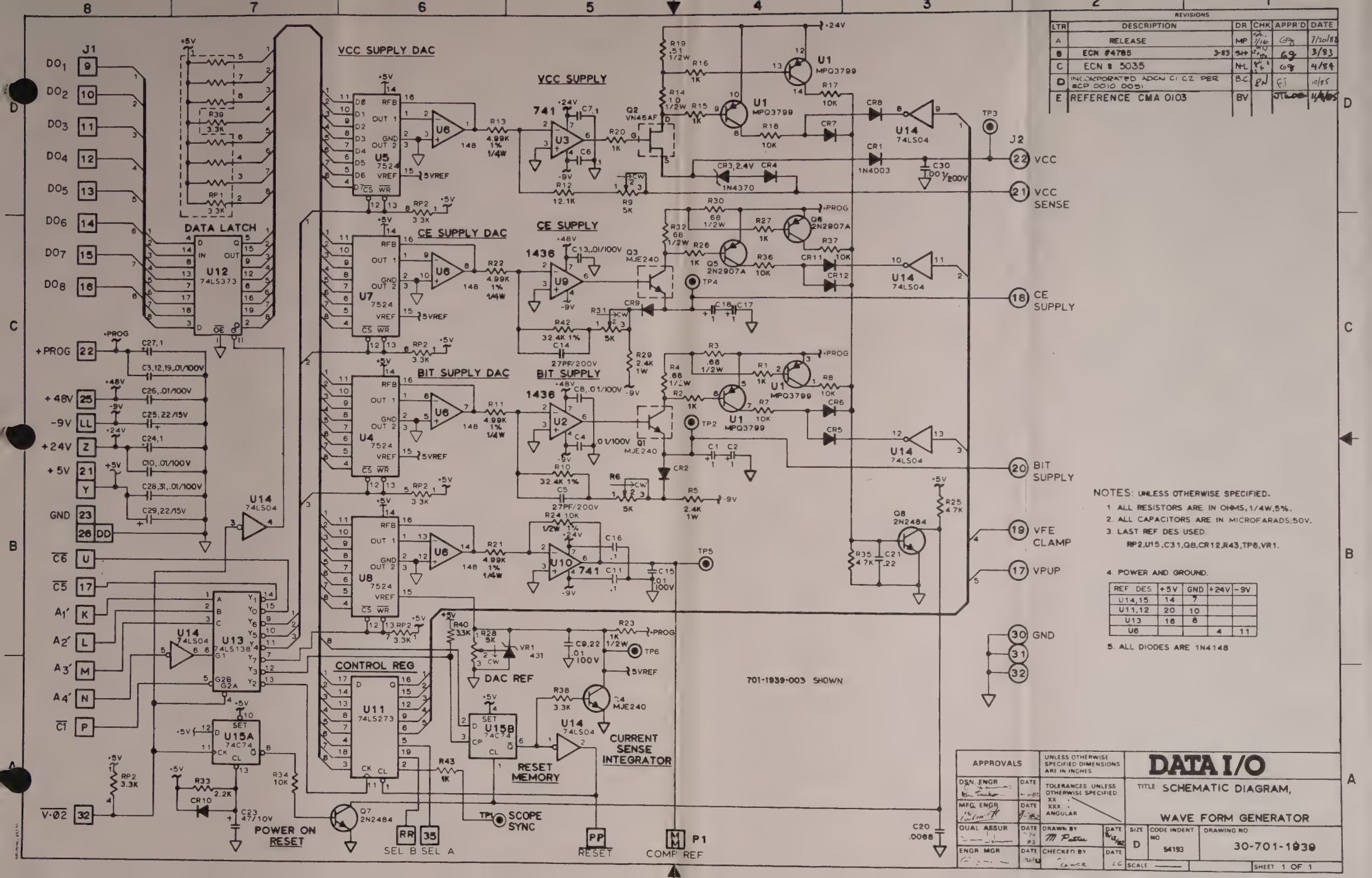
NOTES: UNLESS OTHERWISE SPECIFIED

I. LAST REFERENCE DESIGNATOR USED:

JP 1, J6

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O			
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED		TITLE SCHEMATIC DIAGRAM,			
MFG ENGR	DATE	XX ± XXX ± ANGULAR		MOTHER BOARD			
QUAL ASSUR	DATE	DRAWN BY	DATE	SIZE	CODE INCH	DRAWING NO	
ENGR MGR	DATE	JAEHEE KIM	12/81	D	54193	30-702-1938	
		CHECKED BY	DATE	SCALE		12-17-81 SHEET 1 OF 1	





REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
A	RELEASE	MP	1/16	GF 7/20/88
B	ECN #4785	3-83	5/10	69 3/93
C	ECN # 5035	NH	1/1	69 4/84
D	INCORPORATED ADDN C1 C2 PER BCP 0010 0051	BC	8/1	61 10/85
E	REFERENCE CMA 0103	BV	JT	68 4/85

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REF DES USED.
RP2, U15, C31, Q8, CR12, R43, TP6, VR1.

4. POWER AND GROUND.

REF	DES	+5V	GND	+24V	-9V
U14, 15	14	7			
U11, 12	20	10			
U13	18	8			
U8			4	11	

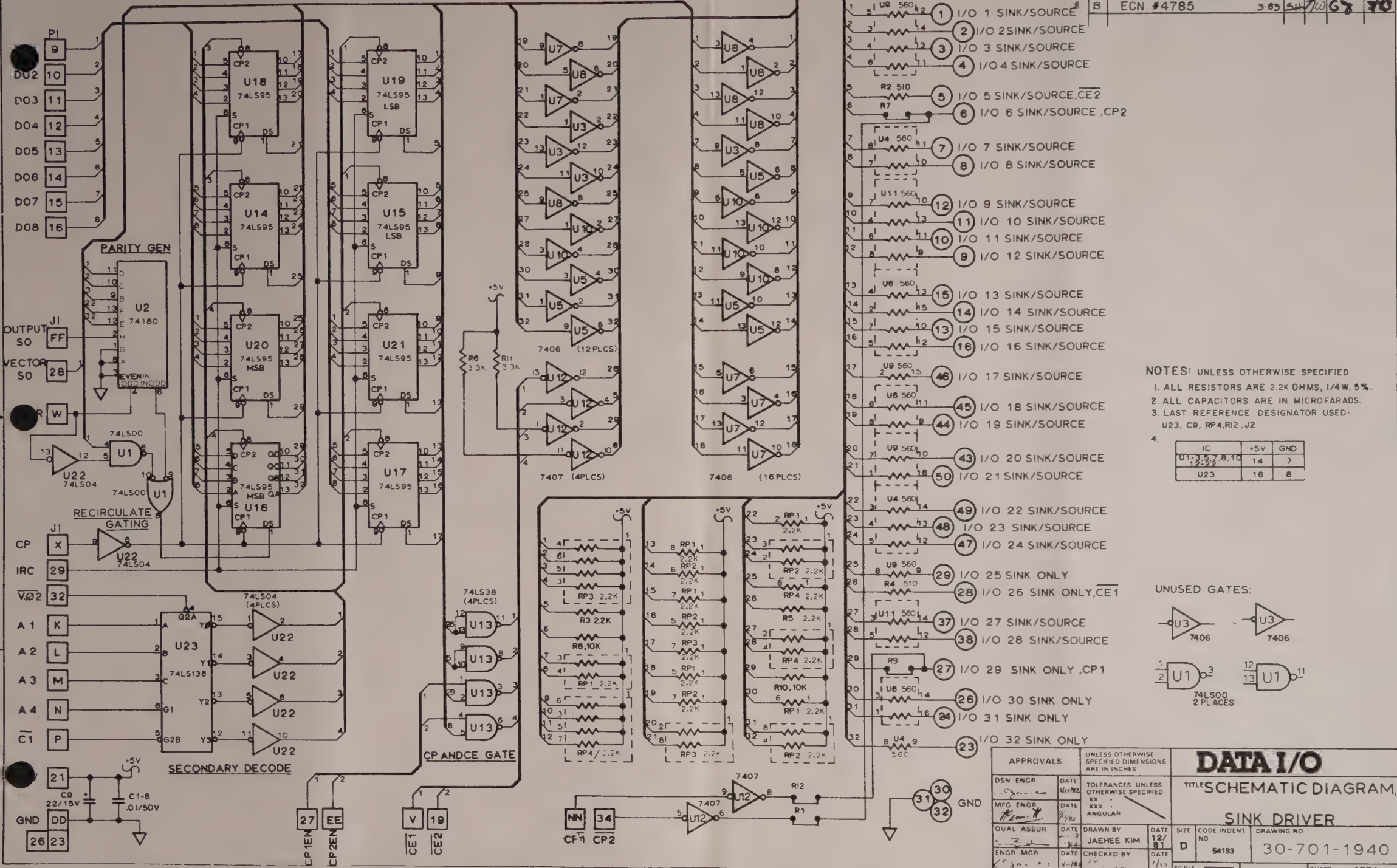
5. ALL DIODES ARE 1N4148

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED		TITLE SCHEMATIC DIAGRAM,	
MFG ENGR	DATE	XX		WAVE FORM GENERATOR	
QUAL ASSUR	DATE	XXX		DRAWING NO	
ENGR MGR	DATE	ANGULAR		30-701-1939	
DRAWN BY		CHECKED BY		SCALE	
DATE		DATE		SHEET 1 OF 1	

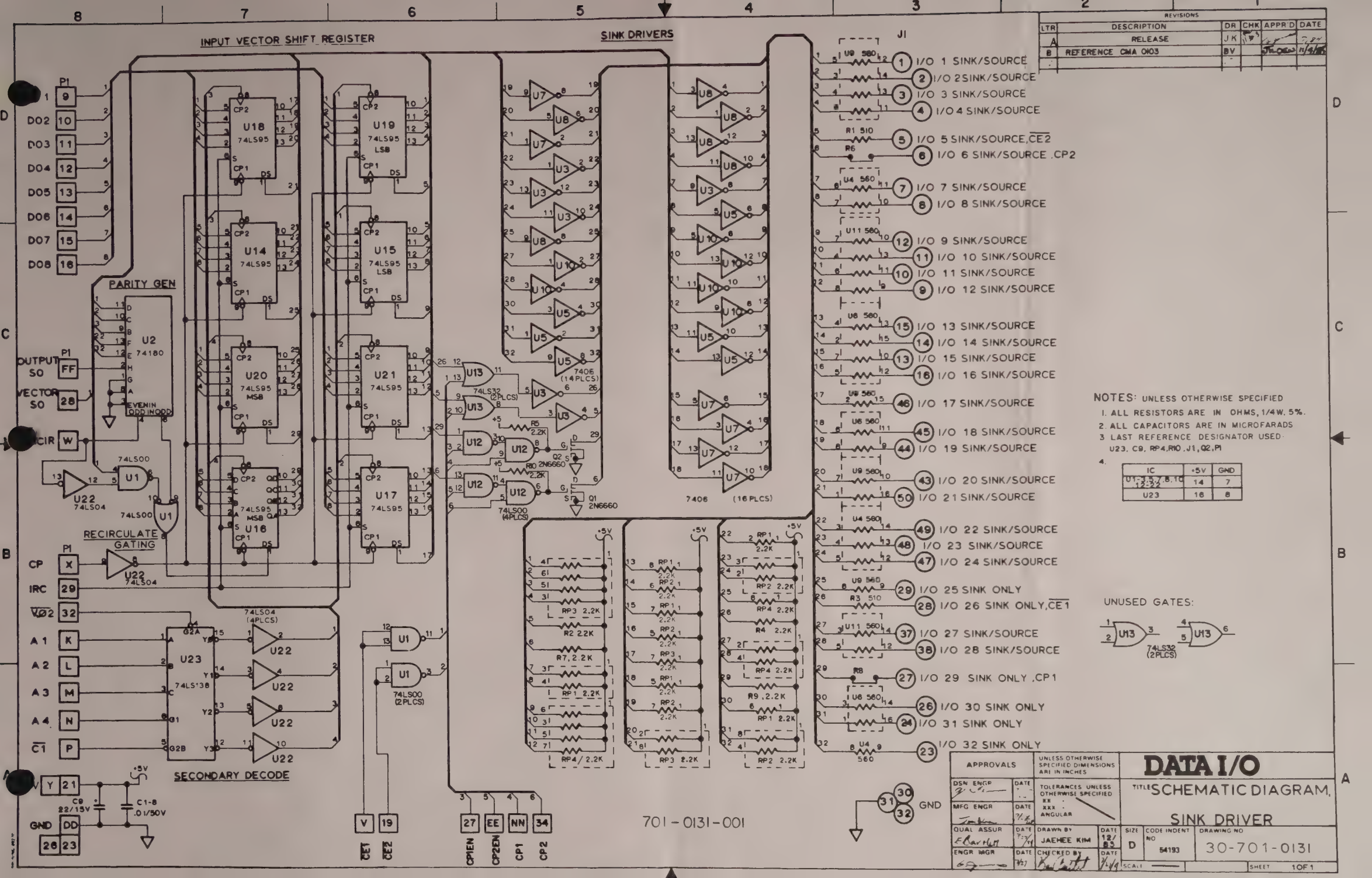


INPUT VECTOR SHIFT REGISTER

SINK DRIVERS



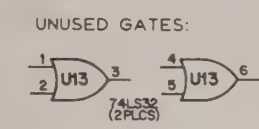




REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D
A	RELEASE	JK		
B	REFERENCE CMA 0103	BV		

- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. LAST REFERENCE DESIGNATOR USED.
 4. U23, C9, RP4, R10, J1, Q2, P1

IC	+5V	GND
U1-15, 18, 19	14	7
U23	16	8



APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES UNLESS OTHERWISE SPECIFIED	
DSW ENGR	DATE	DATE	DRAWN BY	DATE	SIZE
MFG ENGR	DATE	DATE	JAEHEE KIM	DATE	D
QUAL ASSUR	DATE	DATE	DATE	DATE	CODE IDENT
ENGR MGR	DATE	DATE	DATE	DATE	54193
DRAWING NO				DRAWING NO	
30-701-0131				30-701-0131	
SHEET				SHEET	
1 OF 1				1 OF 1	

8

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SOURCE DRIVERS

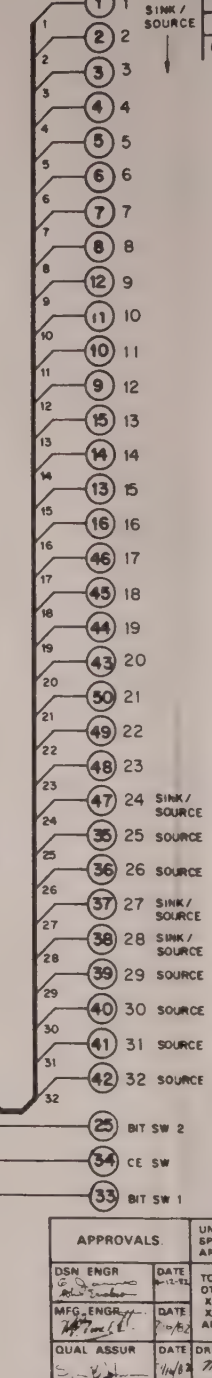
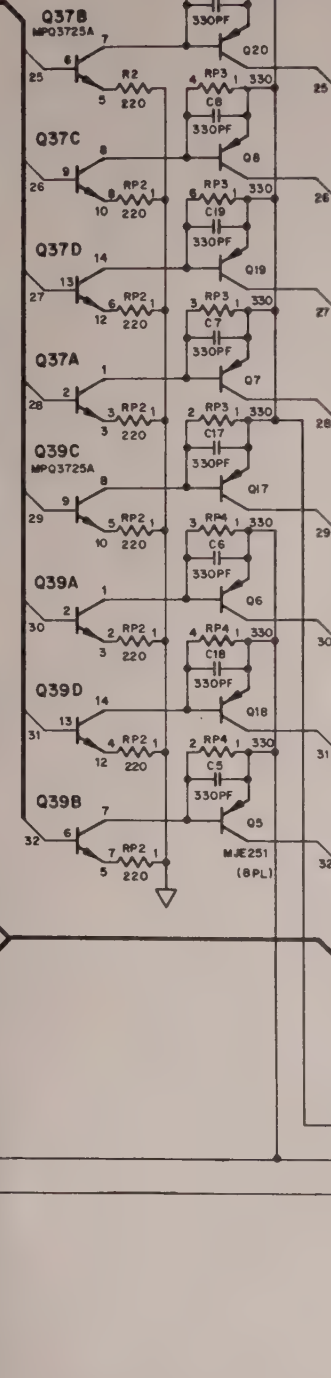
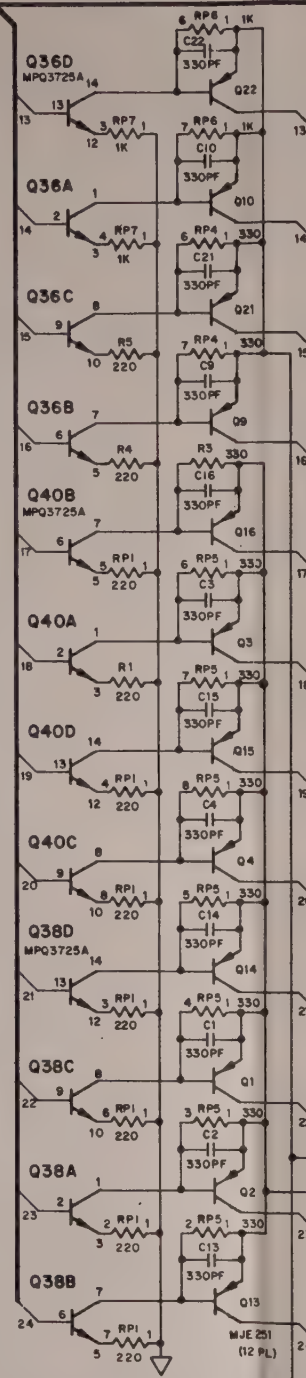
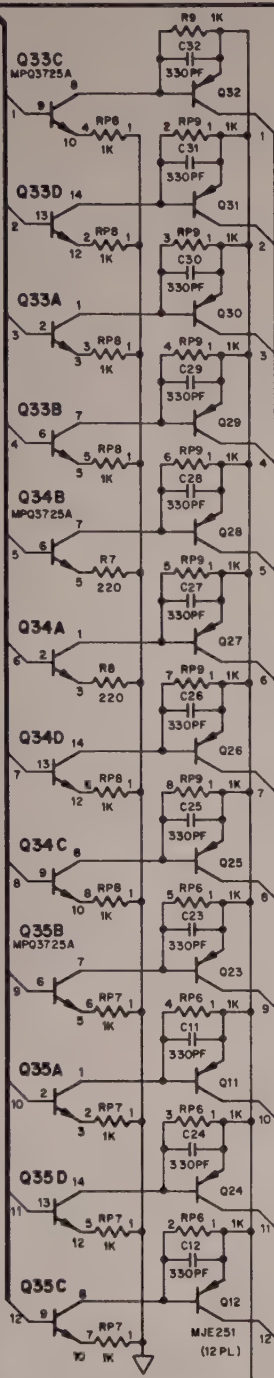
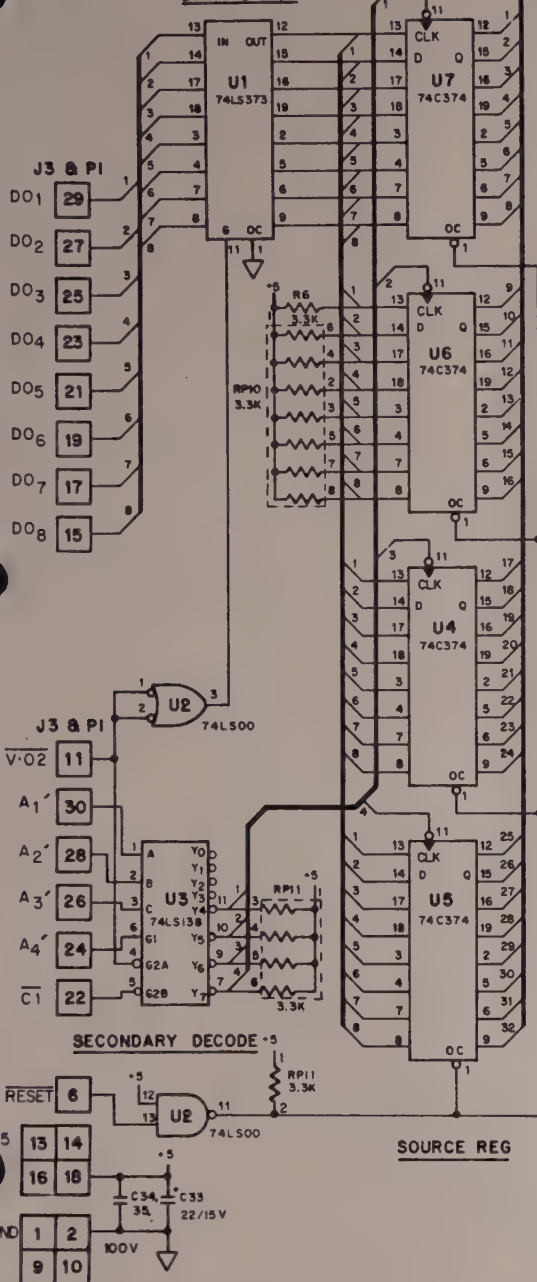
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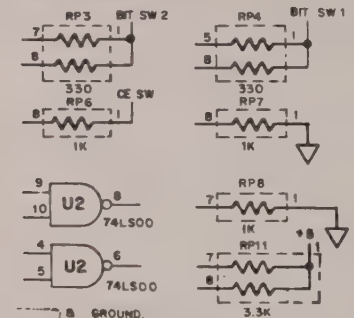
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DATA LATCH



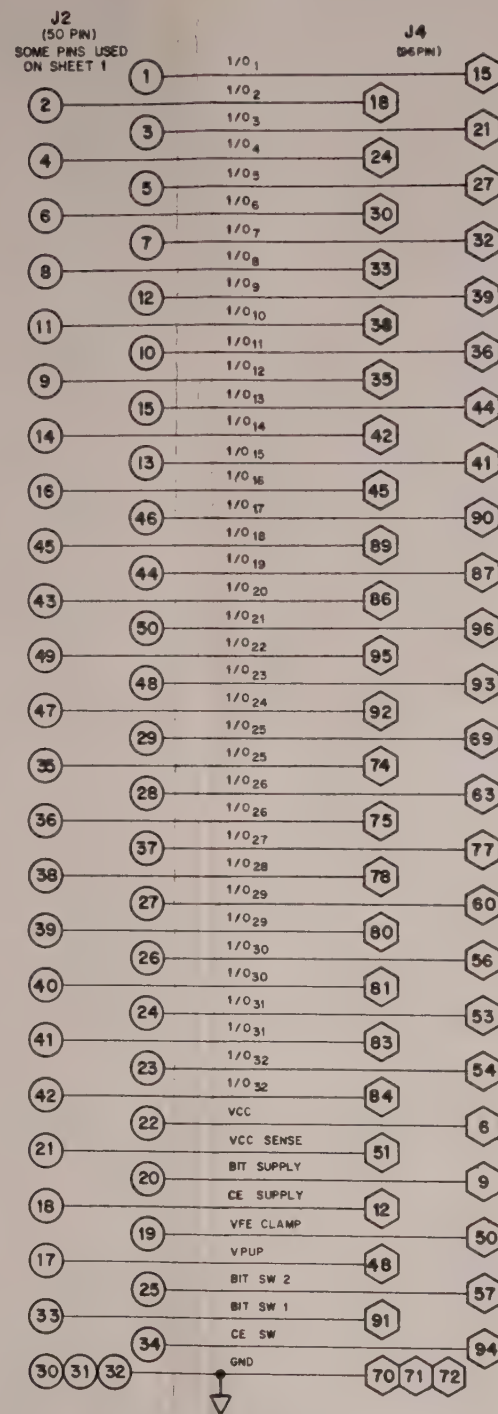
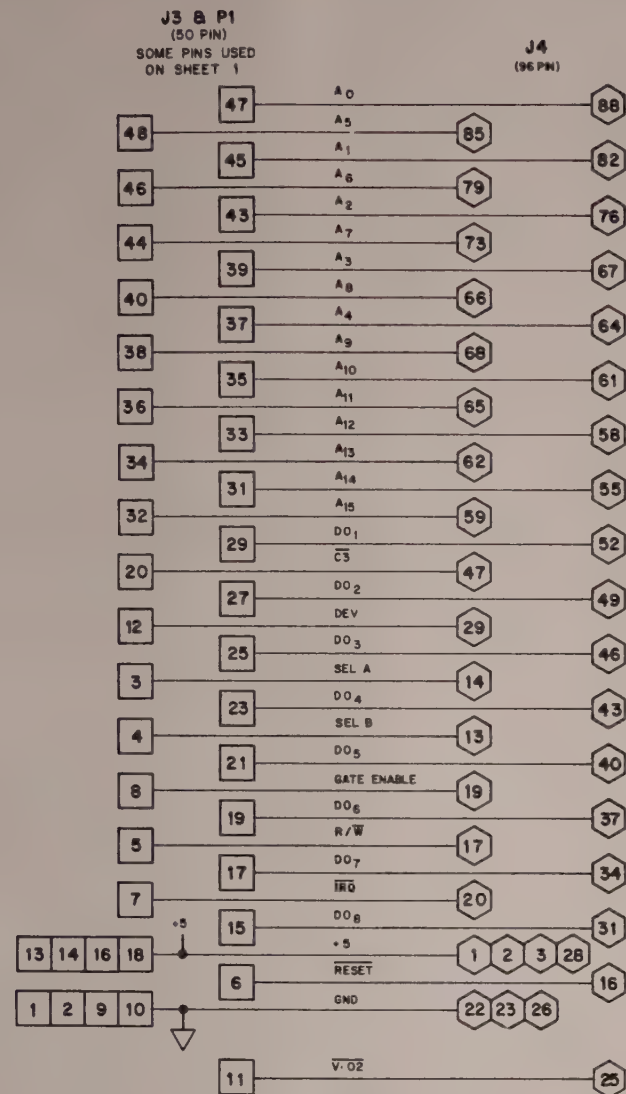
NOTES: UNLESS OTHERWISE SPECIFIED.

- ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
- ALL CAPACITORS ARE IN MICROFARADS, 1KV, 10%.
- LAST REF DES USED
C35, R9, Q40, RP11, U7, J3
- UNUSED DEVICES



REF DES	-5	GND
U1,4-7	20	10
U3	16	8
U2	14	7

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES UNLESS OTHERWISE SPECIFIED		TITLE	
DSN ENGR	DATE	DATE	DATE	DATE	DATE	SCHEMATIC DIAGRAM, PIN DRIVER	
MFG ENGR	DATE	DATE	DATE	DATE	DATE	TITLE	
QUAL ASSUR	DATE	DRAWN BY	DATE	SIZE	CODE IDENT	DRAWING NO	
ENGR MGR	DATE	CHECKED BY	DATE	D	54133	30-702-1943	
SCALE				SHEET 1 OF 2			

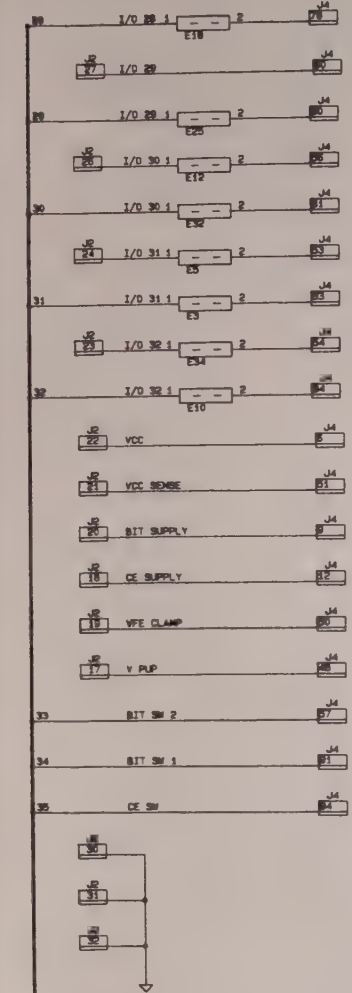
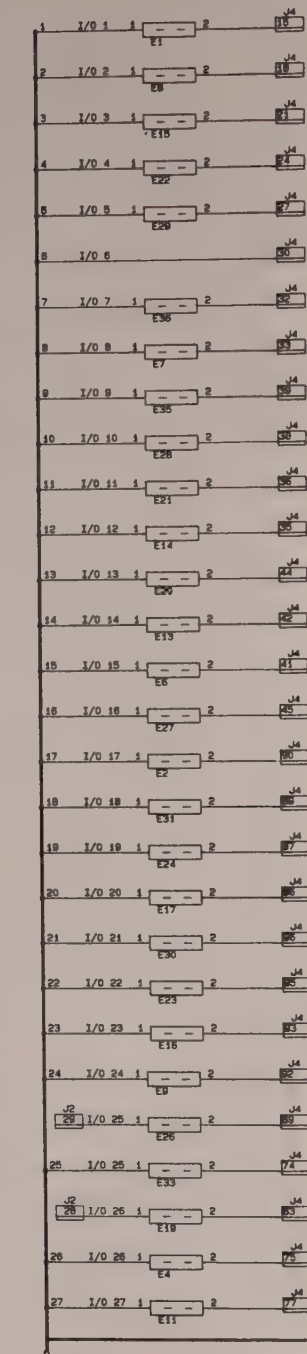
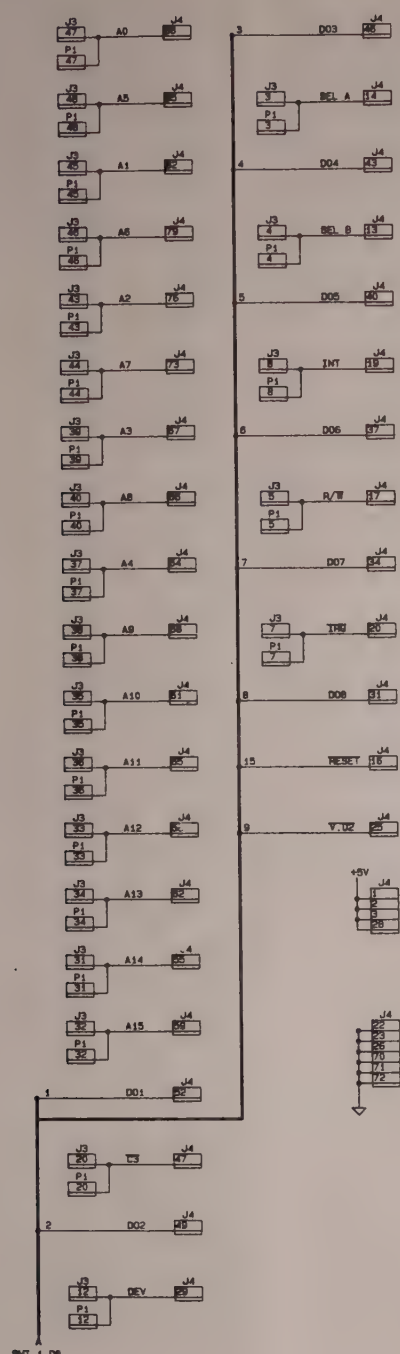


REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
A	SEE SHT 1			
B	ECN #4785	3-83	SV	69 3/83
C	REFERENCE CMA 0103	BV		11/8/80

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O			
DSN ENGR G. J. Jones	DATE 4-12-80	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± ANGULAR		TITLE SCHEMATIC DIAGRAM, PIN DRIVER			
MFG ENGR	DATE			QUAL ASSUR	DATE	DRAWN BY M. J. Jones	DATE 4-12-80
ENGR. MGR	DATE			CHECKED BY J. J. Jones	DATE 4-12-80	SIZE D	CODE IDENT 54193
SCALE				DRAWING NO 30-702-1943			
				SHEET 2 OF 2			





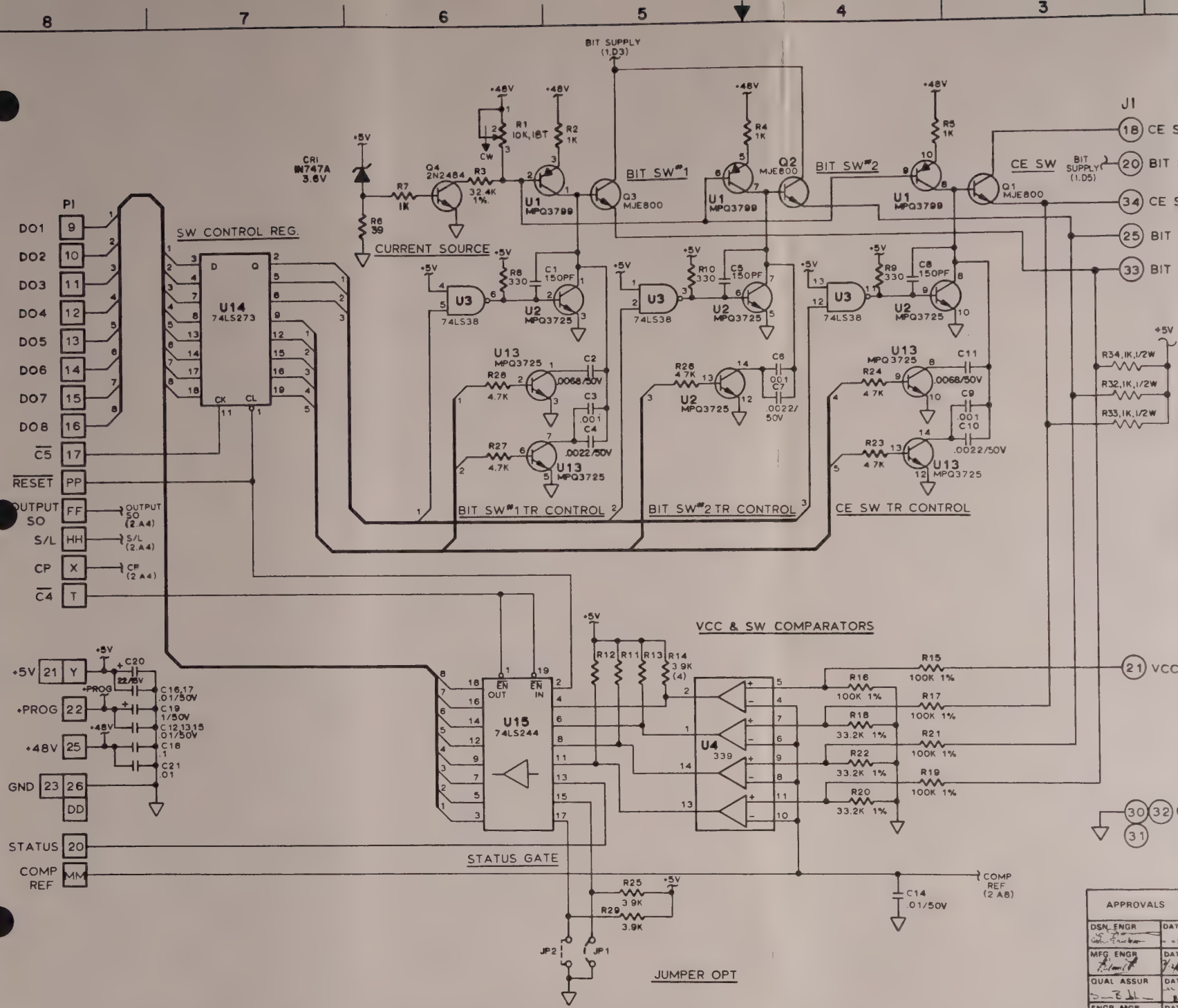


ZONE/LTR		REVISIONS		CM	PE	DATE
A		RELEASE				

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
PROJ. ENG.	TOLERANCES	DECIMALS	ANGULAR	TITLE	
ENG. MGR.	.X ±	.XX ±	.XXX ±	SCHEMATIC DIAGRAM	
		DO NOT SCALE DRAWING		PINDRIVER	
G.C.	DRAWN BY:	SIZE	CODE IDENT NO.	DRAWING NO.	
DATE	CHECKED BY:	D	54193	30-701-0143	
		SCALE		SHEET 2 OF 2	

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REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
A	RELEASE	MP	69	6-30
B	ECN 4677	JK	69	10-20-83
C	ECN 4705	JP	69	1-83
D	ECN 4785	SH	69	3-83
E	INCORPORATED ADDN D1,D2 PER EGP 0010, 0051	B.C.	69	ref: des
F	REFERENCE CMA#0103	BV	ES	ES 5/1/87

- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS 1/4W, 5%.
 2. ALL CAPACITORS ARE IN MFD, 100V.
 3. LAST REF DES USED
R34, C21, JP2, Q7, CR1, U21, J2
 4. POWER AND GROUND.

REF DES	+5	GND	WPROG
U3	14	7	
U4-U12		12	3
U14, 15	20	10	
U16, 18, 21, 19	16	8	

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O			
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED		TITLE SCHEMATIC DIAGRAM,			
MFG ENGR	DATE	XX ?		T/RISE COMPARATOR			
QUAL ASSUR	DATE	DRAWN BY	DATE	SIZE	CODE	IDENT	DRAWING NO
ENGR MGR	DATE	CHECKED BY	DATE	D	54133		30-701-1941
SCALE						SHEET 1 OF 2	

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
F	SEE SMT 1	MP	JL	69 6-30

COMPARATORS

OUTPUT SHIFT REG.

JL

I/O

1 SINK/SOURCE

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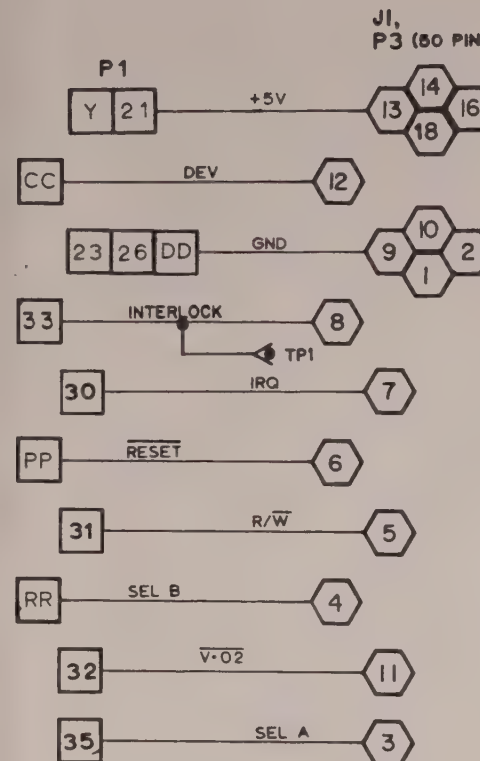
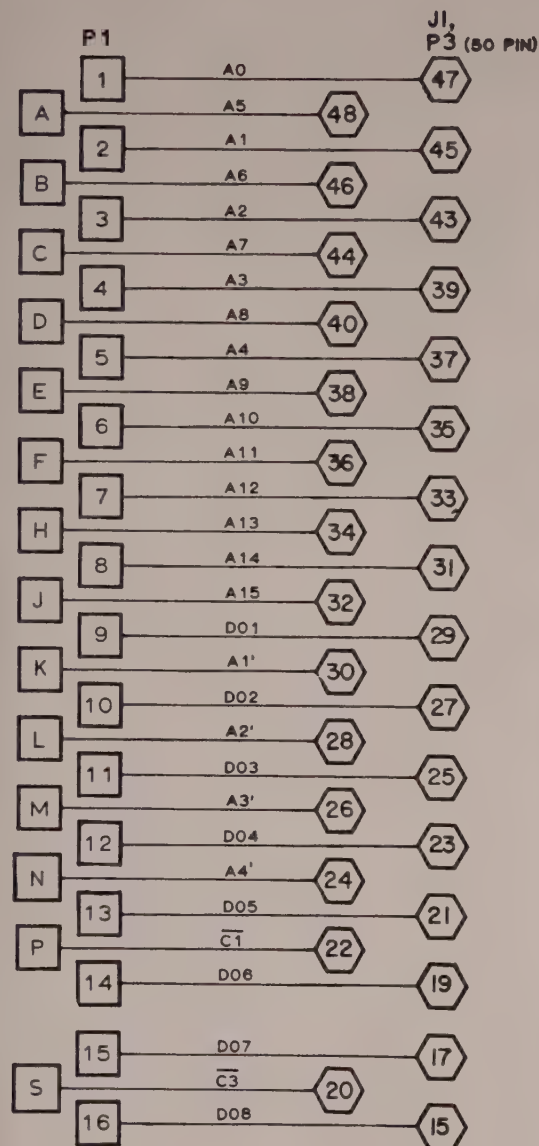
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LTR	DESCRIPTION	DR	CHK	APPR	DATE
A	RELEASE	R.B.	3/77	QY	7/12/82
B	ECN 4685	CL	3/82	QY	7/11/82
C	ECN 54785	SH	3/82	QY	3/83
D	REFERENCE CMA 0103	BV		Stacy	11/4/85

D

C

B

A

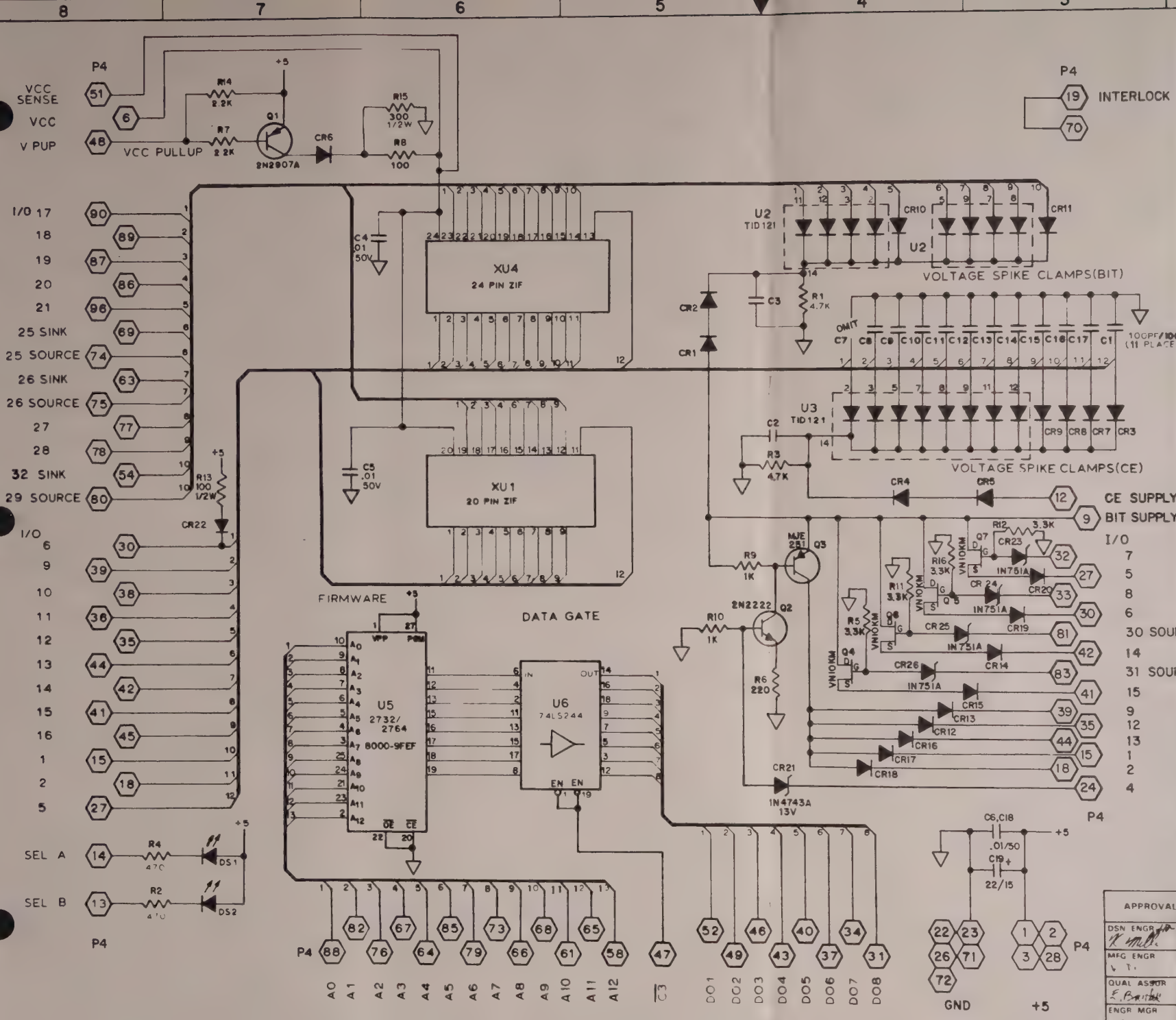


NOTES:

1. LAST REFERENCE DESIGNATOR USED:
P3, J1, TPI

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
DSN ENGR R. BENN	DATE 6-9-82	TOLERANCES UNLESS OTHERWISE SPECIFIED XX : XXX : ANGULAR		TITLE SCHEMATIC DIAGRAM, EXTENDER BOARD 50/72	
MFG ENGR R. BENN	DATE 7-1-82	DRAWN BY R. BENN	DATE 7-1-82	SIZE C	CODE IDENT 54193
QUAL ASSUR R. BENN	DATE 7-1-82	CHECKED BY R. BENN	DATE 7-1-82	DRAWING NO 30-701-1944	
ENGR MGR R. BENN	DATE 7-1-82	SCALE			
SHEET 1 OF 1					





		REVISIONS			
LTR	DESCRIPTION	DR	CHK	APPR	DATE
A	RELEASE	dh	5/14	HA	5-9-68
B	INCRP. ADCN B1 PER ECP 0044	dh	4/1	4m	5-27-68

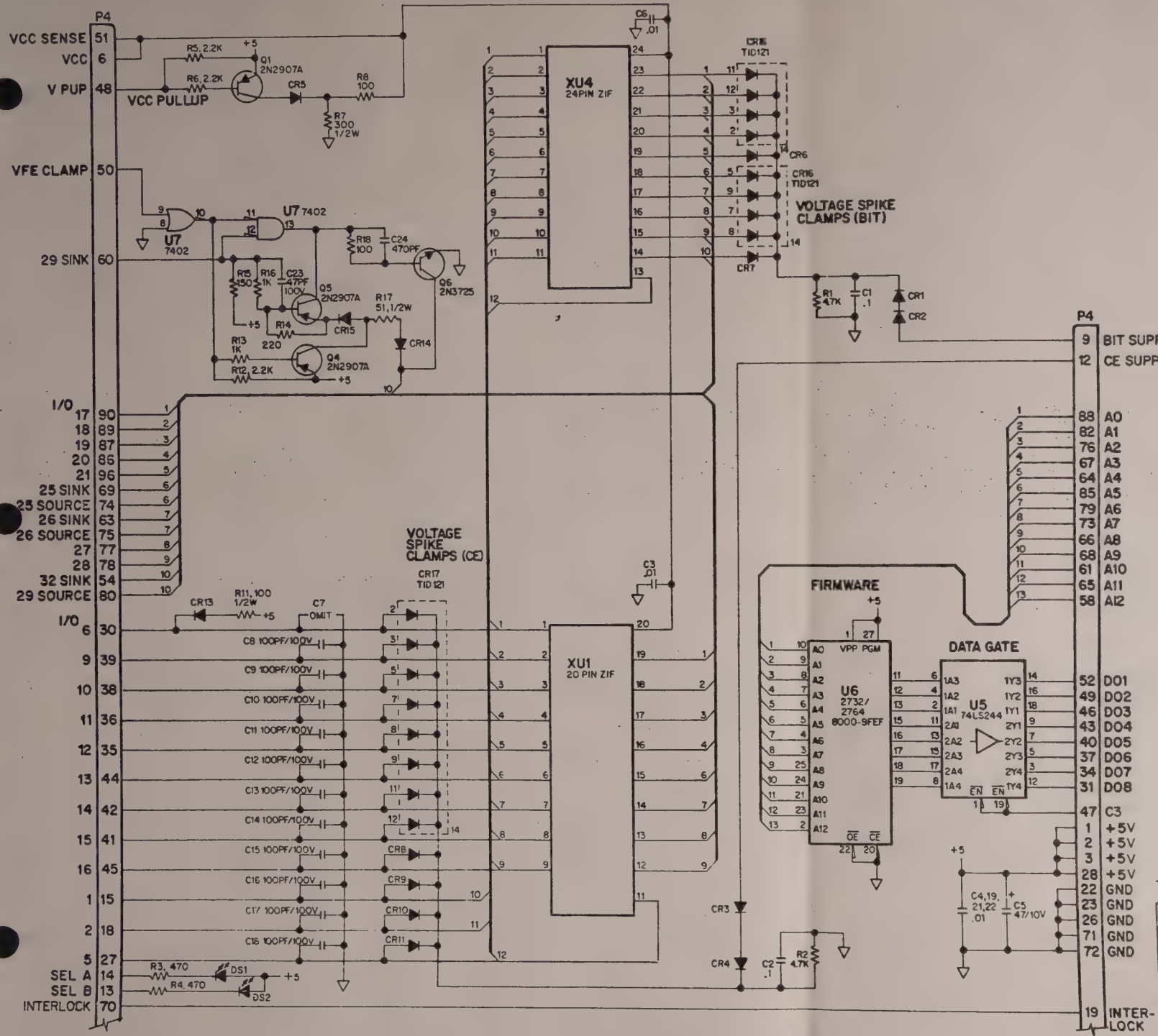
- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS, .1, .50V.
 3. LAST REFERENCE DESIGNATOR USED:
C19, CR22, DS2, P4, R16, U6, Q7.
 4. ALL DIODES 1N4148.

5. POWER & GROUND.

REF DES	+5	GND
XU4	-	12
XU1	-	10
U6	20	10
U5	20, 28	14

P/N 701-0130-002

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O			
DSN ENGR	DATE	DESIGNED BY	DATE	TITLE SCHEMATIC DIAGRAM, TEST PROG ADAPTER			
MFG ENGR	DATE	OTHER USE SPECIFIED	DATE				
QUAL ASSUR	DATE	ANGULAR	DATE				
ENGR MGR	DATE		DATE				
DRAWN BY		CHECKED BY		SIZE	CODE IDENT	DRAWING NO	
L. M. B.		J. M. B.		D	54193	30-701-0130	
1/4/68		1/4/68		NONE		SHEET 1 OF 1	



ZONE/LTR		REVISIONS				CHK		CM		FE		DATE	
		A	RELEASE										

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
- ALL CAPACITORS ARE IN MICROFARADS.
- ALL CAPACITORS ARE 50V.
- ALL DIODES ARE IN4148.
- LAST REFERENCE DESIGNATOR USED: U7, R18, DS2, CR17, C24, P4, Q6.

POWER AND GROUND:		
REFERENCE DESIGNATOR	+5	GROUND
XU1	—	10
XU4	—	12
U5	20	10
XU6	26,28	14
U7	14	7

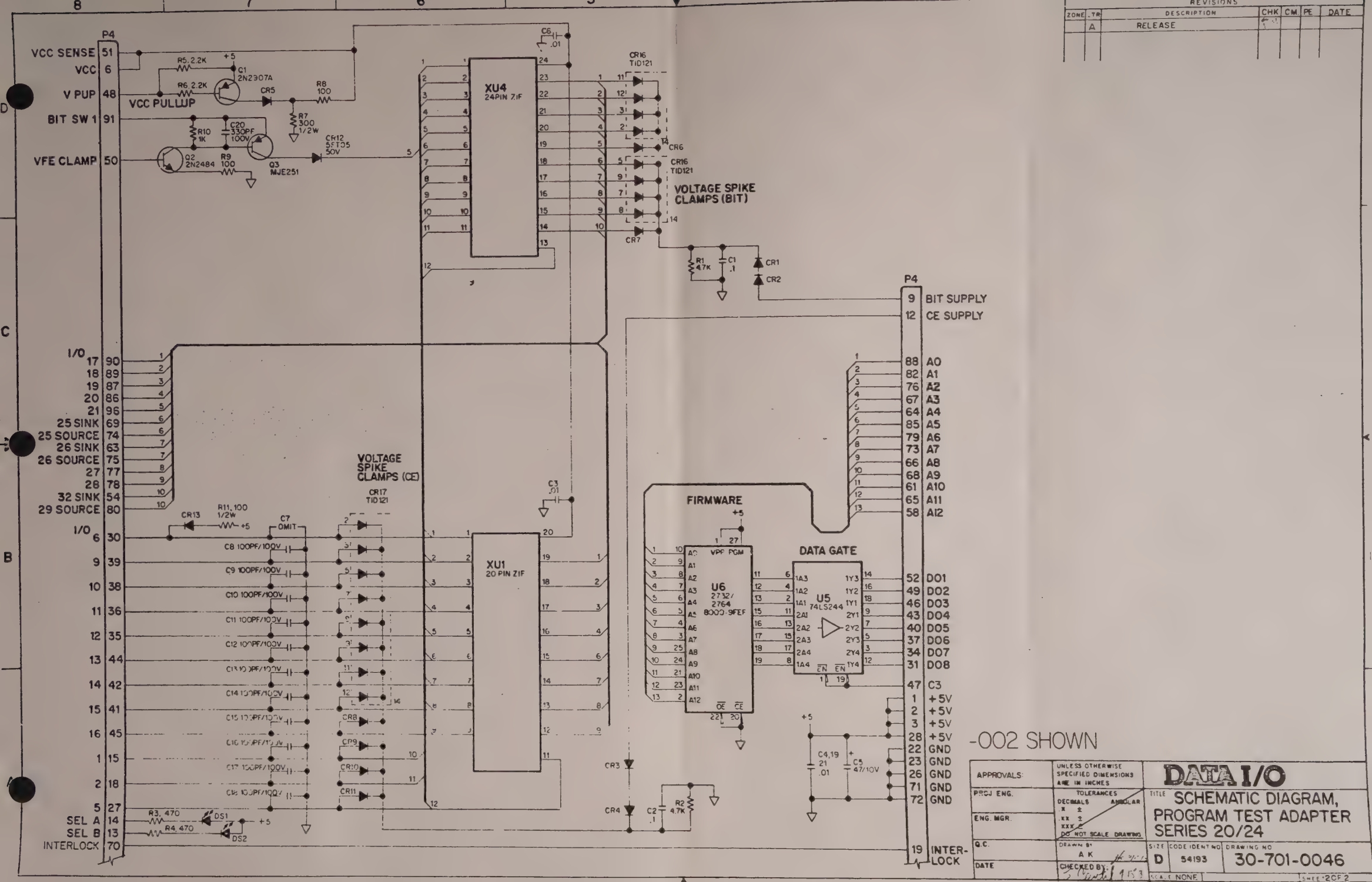
- UNUSED GATES:

U7 7402, 2 PLACES
- REFERENCE DESIGNATORS NOT USED ON -001: R9, R10, C20, CR12, Q2, Q3, U2, U3.
- REFERENCE DESIGNATORS NOT USED ON -002: U7, R12, R13, R14, R15, R16, R17, R18, C22, C23, C24, CR14, CR15, Q4, Q5, Q6, U2, U3.

-001 SHOWN

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES DECIMALS ANGULAR		TITLE	
PROJ. ENG.	E.L. SWEENEY	DO NOT SCALE DRAWING				DATA I/O	
ENG. MGR.	E.L. SWEENEY					SCHEMATIC DIAGRAM, PROGRAM TEST ADAPTER	
Q.C.						SERIES 20/24	
DATE						D 54193 30-701-0046	
DRAWN BY		CHECKED BY:		SIZE CODE IDENT NO DRAWING NO		SCALE NONE	
A.K.						SHEET OF 2	

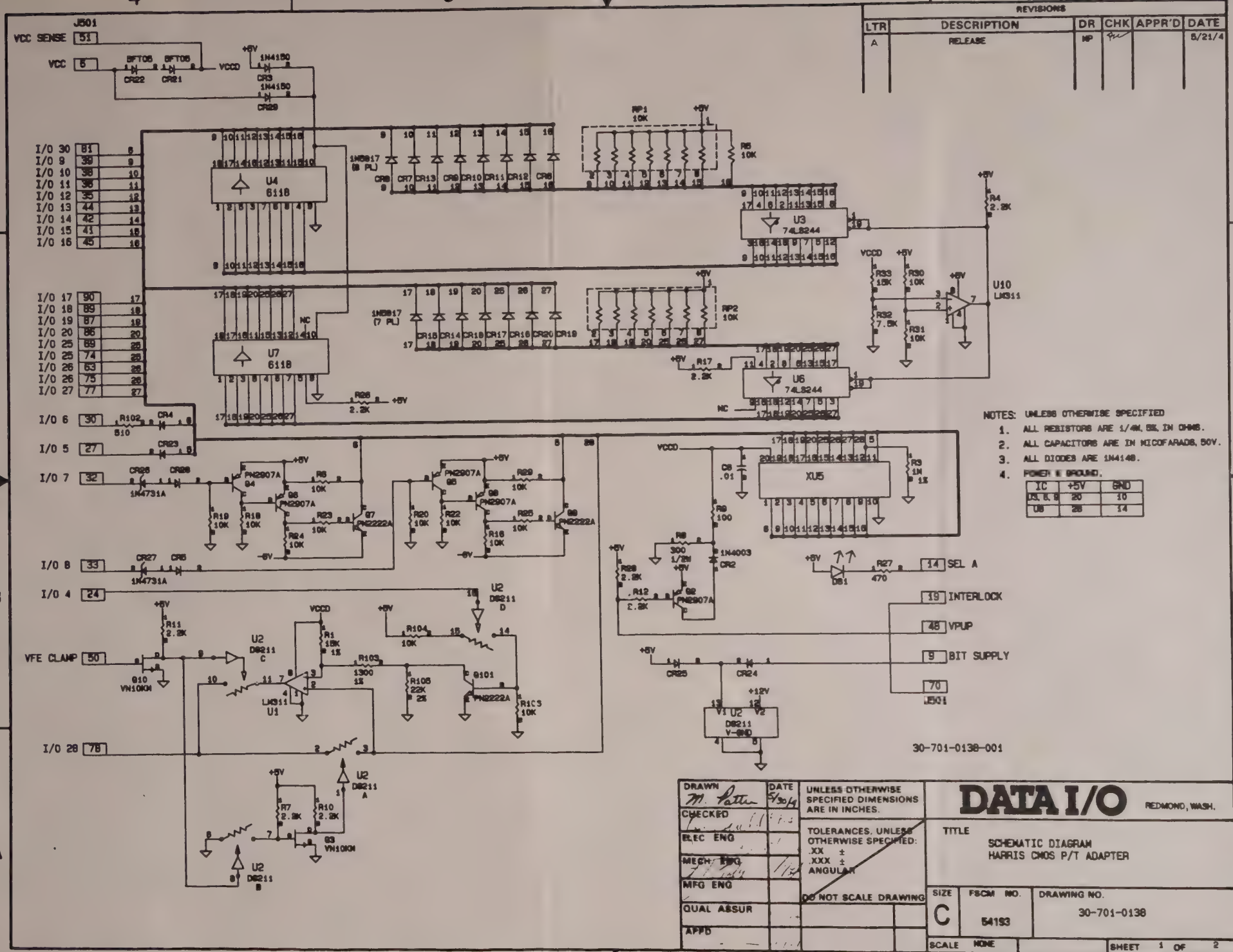




-002 SHOWN

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	TITLE	
PROJ. ENG.	TOLERANCES	DECIMALS ANGULAR	SCHEMATIC DIAGRAM, PROGRAM TEST ADAPTER SERIES 20/24	
ENG. MGR.	XX ±	XX ±	DO NOT SCALE DRAWING	
G.C.	DRAWN BY	A K	SIZE	CODE IDENT NO
DATE	CHECKED BY	9/5/83	D	54193
		SCALE NONE	DRAWING NO 30-701-0046	





J501

VCC SENSE	51
VCC	5
I/O 9	39
I/O 10	38
I/O 11	36
I/O 12	35
I/O 13	44
I/O 14	42
I/O 15	41
I/O 16	45

I/O 17	90
I/O 18	89
I/O 19	87
I/O 20	86
I/O 25	89
I/O 26	74
I/O 27	77

I/O 6	30
I/O 5	27

I/O 7	32
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VFE CLAMP	50
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I/O 28	78
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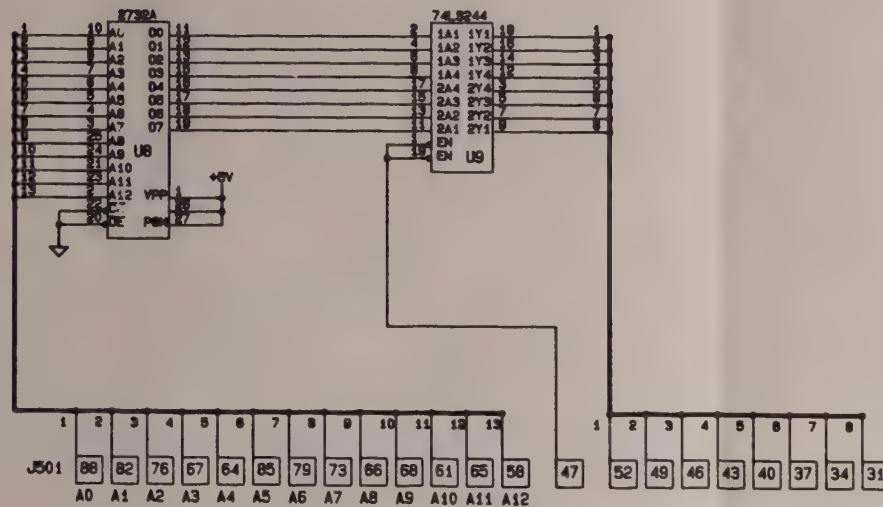
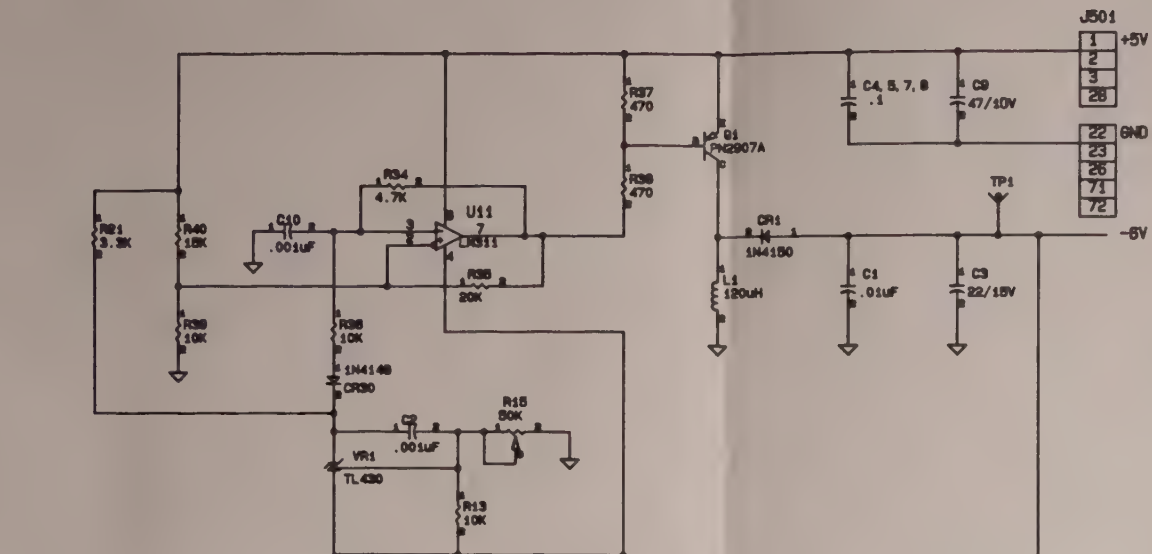
- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W, 5%, IN OHMS.
 2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
 3. ALL DIODES ARE 1N4148.
 4. POWER & GROUND.

IC	+5V	GND
U1, 5, 6	20	10
U8	28	14

30-701-0138-001

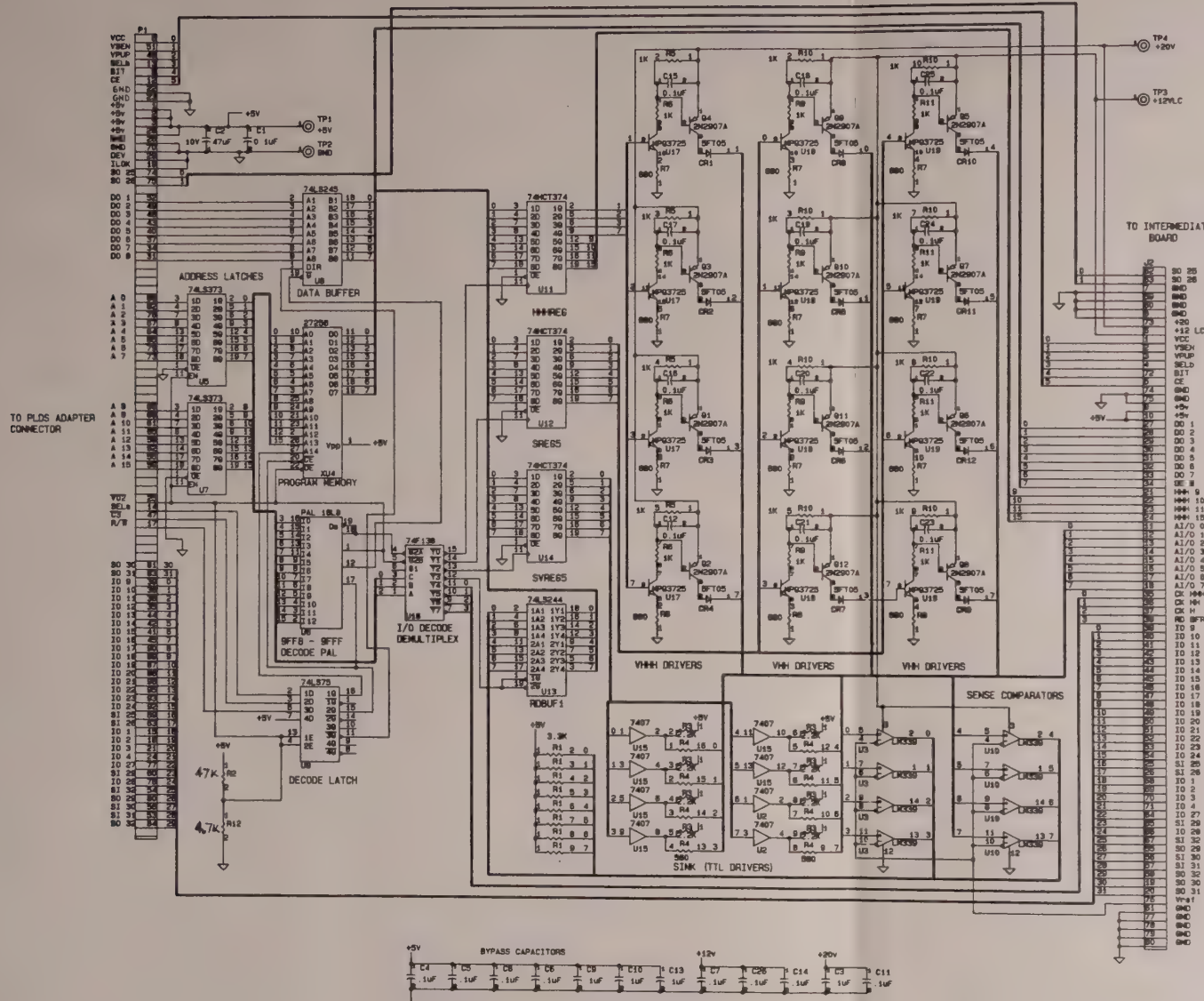
DRAWN <i>M. Latta</i>	DATE 5/30/4	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		DATA I/O REDMOND, WASH.	
CHECKED <i>[Signature]</i>		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR		TITLE SCHEMATIC DIAGRAM HARRIS CMOS P/T ADAPTER	
ELEC ENG		DO NOT SCALE DRAWING		SIZE C	FSCM NO. 54193
MECH ENG				DRAWING NO. 30-701-0138	
MFG ENG					
QUAL ASSUR					
APPD					
SCALE NONE				SHEET 1 OF 2	

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D
A	RELEASE	MP		
				5/21/4

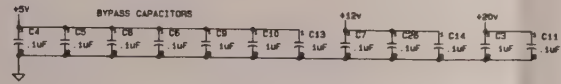
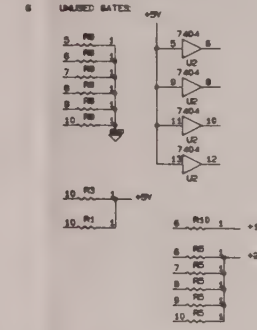


DRAWN <i>M. Patton</i>		DATE 5/20/4	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		DATA I/O REDMOND, WASH.
CHECKED <i>L. J. Patton</i>			TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR		
MECH ENG			DO NOT SCALE DRAWING		TITLE SCHEMATIC DIAGRAM HARRIS CMOS P/T ADAPTER
MFG ENG					
QUAL ASSUR					SIZE C
APPD					FSCM NO. 54193
					DRAWING NO. 30-701-0138
					SCALE NONE
					SHEET 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DR	CHK APPR'D DATE
A	RELEASE		
B	INCCORP. AI PER EPO101	EC	11/78



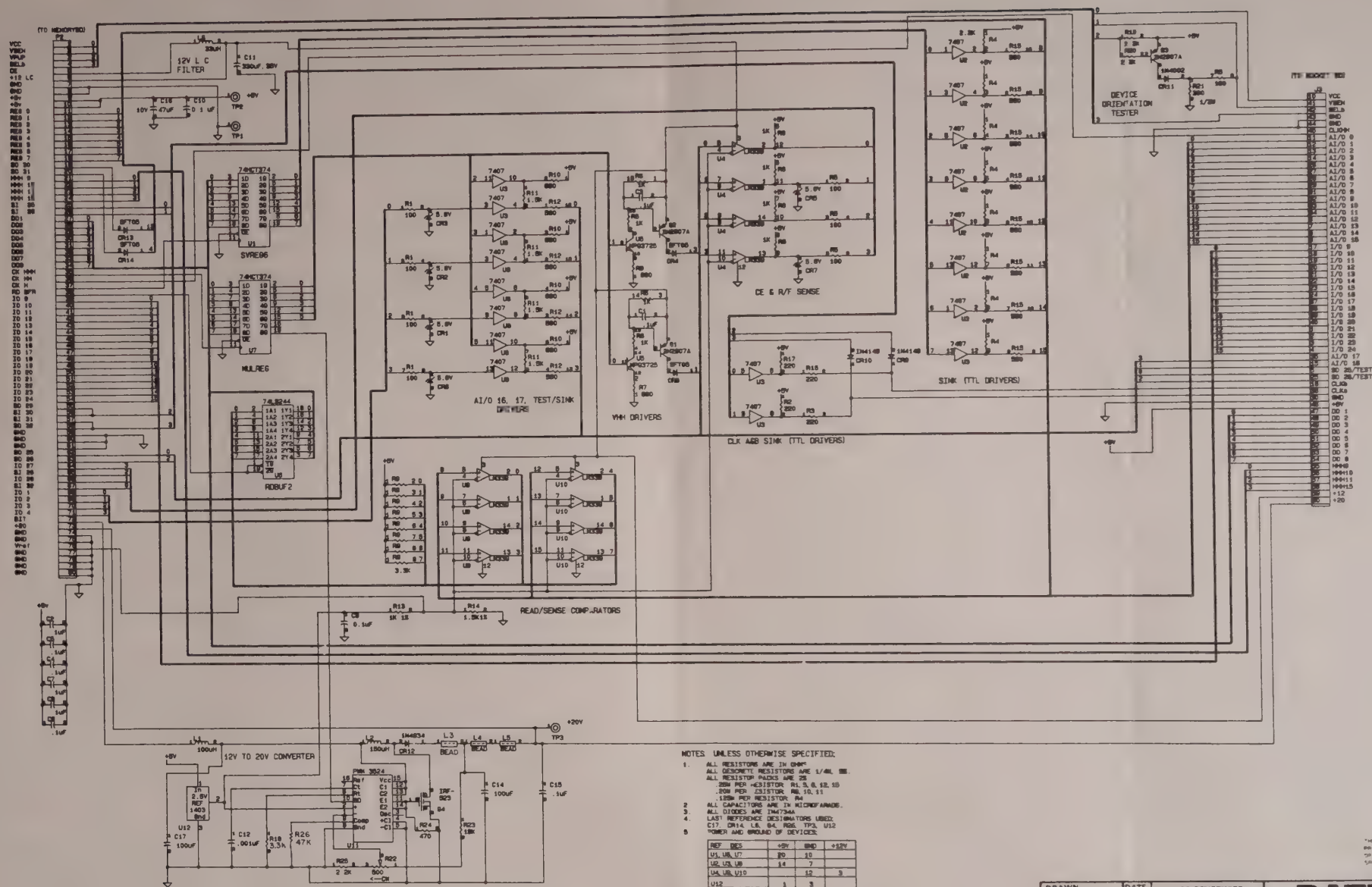
- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL RESISTORS ARE IN OHMS
 - ALL DISCRETE RESISTORS ARE 1/4W 5%
 - ALL RESISTOR PACKS ARE 25
 - 100 PER RESISTOR: R1, 5, 7, 8, 10
 - 100 PER RESISTOR: R3
 - 100 PER RESISTOR: R4, 8, 9, 11
 - ALL CAPACITORS ARE IN MICROFARADS
 - LAST REFERENCE DESIGNATORS USED:
 - CR1, CR2, R12, R12, TR1, U19
 - REFERENCE DESIGNATORS NOT USED:
 - U1
- POWER AND GROUND OF DEVICES
- | REF | DES | +5V | GND | +12V |
|--------------------|-----|-----|-----|------|
| U2, U15 | 14 | 7 | | |
| U3, U10 | 12 | 3 | | |
| U4 | 28 | 14 | | |
| U5, U6, U7, U8 | 20 | 10 | | |
| U11, U12, U13, U14 | | | | |
| U9 | 5 | 12 | | |
| U16 | 16 | 8 | | |



701-0149-001

DRAWN T. 107	DATE 11/78	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O REDMOND, WASH.
CHECKED 1	DESIGNED B. S.	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	
elec ENG 1	MECH. ENG 1	DO NOT SCALE DRAWING	TITLE SCHEMATIC I/O MEMORY & ADDRESS
MFG ENG 1	QUAL ASSUR 1		SIZE D FSCM NO 54193 DRAWING NO 30-701-0149
APPRO 1			SCALE NONE SHEET 1 OF 1

LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	11/1/78	11/1/78	LR	11/1/78
B	INCRP. ADIN #A1 PER ECP#0101	11/1/78	11/1/78	LR	6/14/78



NOTES UNLESS OTHERWISE SPECIFIED:

- ```

1. ALL RESISTORS ARE IN OHMS
 ALL DISCRETE RESISTORS ARE 1/4W. 5%
 ALL RESISTOR PACKS ARE 25
 .25W PER RESISTOR R1, 3, 8, 12, 10
 .20W PER RESISTOR R6, 10, 11
 .125W PER RESISTOR R4

2. ALL CAPACITORS ARE IN MICROFARADS.

3. ALL DIODES ARE 1N4734A

4. LAST REFERENCE DESIGNATORS USED:
 C17, C14, L8, B4, R62, TP3, U32

5. POWER AND GROUND OF DEVICES.

```

| REF | DES     | +5V | 0V | +12V |
|-----|---------|-----|----|------|
| U1  | U1, U7  | 10  | 10 |      |
| U2  | U3, U8  | 14  | 7  |      |
| U4  | U2, U10 |     | 12 | 5    |
| U12 |         | 1   | 3  |      |

6 UNLINED COMPONENTS:



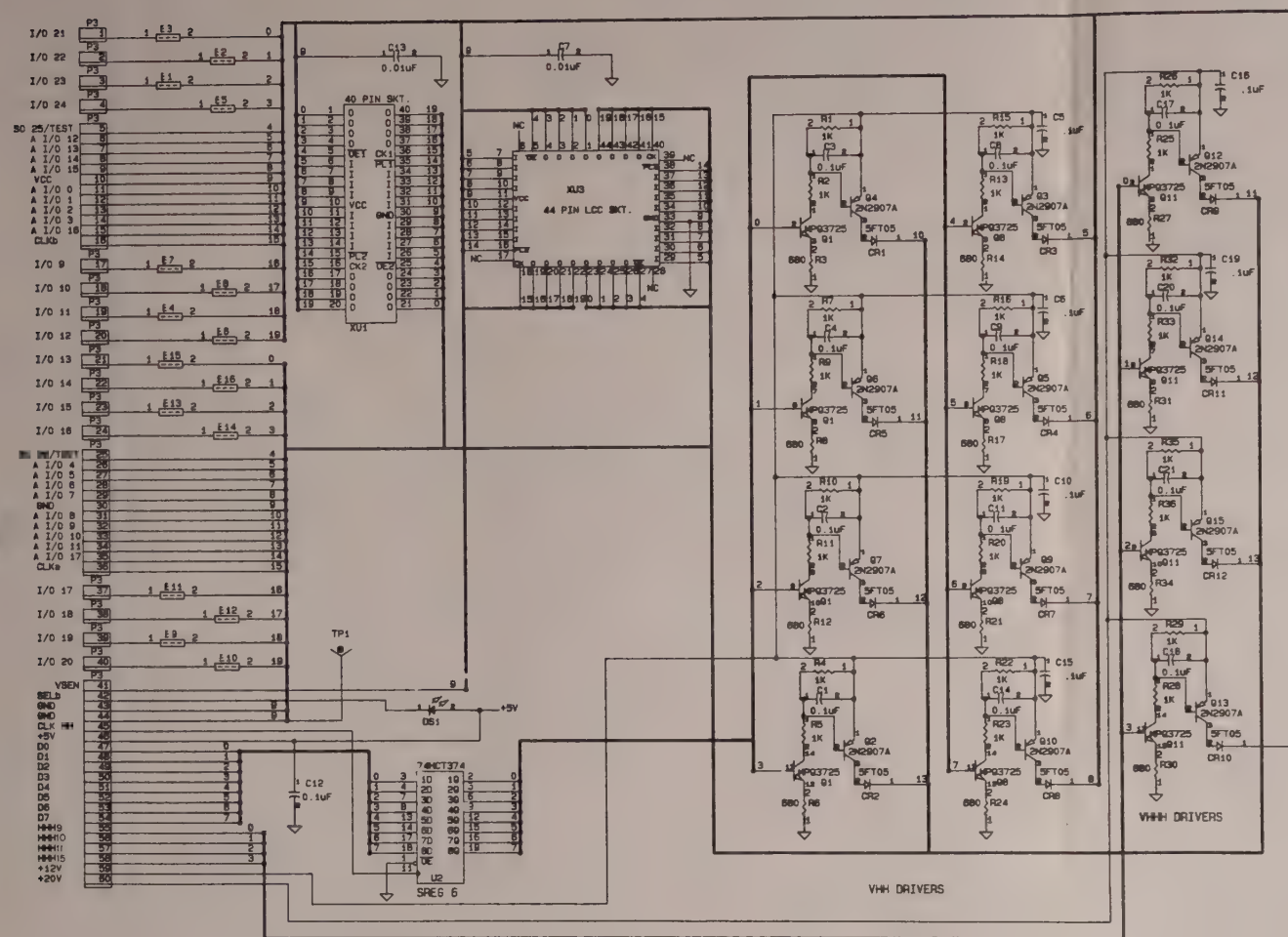
- [illegible]

7. REFERENCE DESIGNATOR NOT USED: C13

|                     |  |                                                               |  |                                                        |                  |                                  |  |
|---------------------|--|---------------------------------------------------------------|--|--------------------------------------------------------|------------------|----------------------------------|--|
| DRAWN<br>T. LOTH    |  | DATE<br>11/1/54                                               |  | UNLESS OTHERWISE SPECIFIED<br>DIMENSIONS ARE IN INCHES |                  | <h1>DATA I/O</h1> REDMOND, WASH. |  |
| CHECKED<br>J. L.    |  | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX<br>XXX<br>ANGULAR |  | TITLE<br>SCHEMATIC DIAGRAM<br>INTERMEDIATE BOARD       |                  |                                  |  |
| MFG ENG<br>J. L.    |  | DO NOT SCALE DRAWING                                          |  | SIZE<br>D                                              | FSCM NO<br>54193 | DRAWING NO<br>30-701-014B        |  |
| MFG ENG<br>J. L.    |  |                                                               |  |                                                        |                  |                                  |  |
| QUAL ASSUR<br>J. L. |  |                                                               |  |                                                        |                  |                                  |  |
| APPROVED<br>J. L.   |  |                                                               |  | SCALE NONE                                             |                  | SHEET 1 OF 1                     |  |



| LTR |  | DESCRIPTION |  | REVISIONS |  | DR | CHK | APPR'D | DATE     |
|-----|--|-------------|--|-----------|--|----|-----|--------|----------|
| A   |  | RELEASE     |  |           |  |    |     |        | 11/17/79 |



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. OMITTED
4. LAST REFERENCE DESIGNATOR USED.

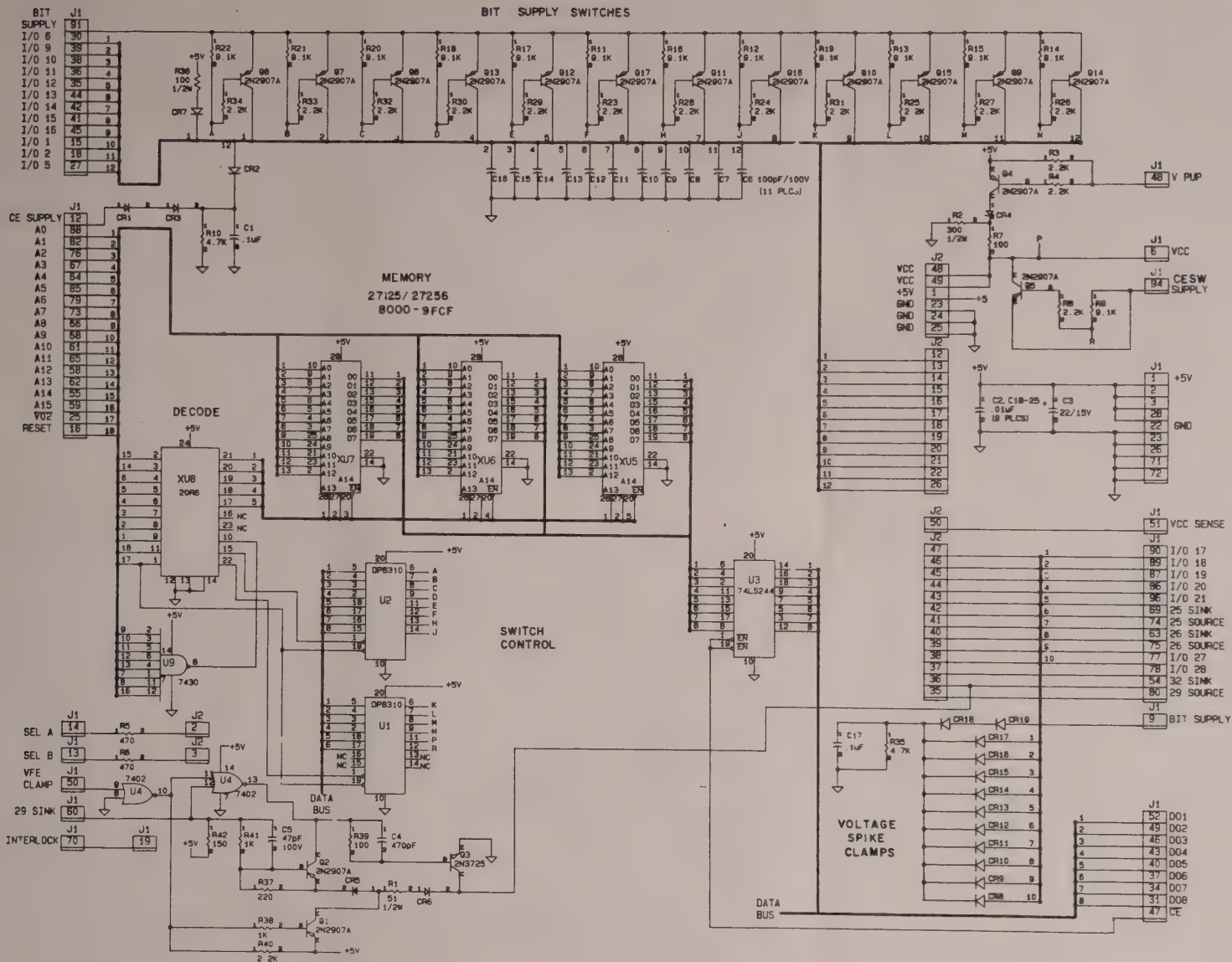
P3, R36, CR12, C21, Q15, E16, XU3, TP1, DS1.

P/N 701-0009-001  
-002

|                            |  |             |  |                                                                   |  |                                          |  |
|----------------------------|--|-------------|--|-------------------------------------------------------------------|--|------------------------------------------|--|
| DRAWN<br>J. H. H. 1/8      |  | DATE<br>1/8 |  | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES               |  | <h1>DATA I/O</h1> REMONIC WASH           |  |
| CHECKED<br>J. H. H. 1/8    |  | DATE<br>1/8 |  | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX ±<br>XXX ±<br>ANGULAR |  |                                          |  |
| ELEC ENG<br>J. H. H. 1/8   |  | DATE<br>1/8 |  | DO NOT SCALE DRAWING                                              |  | TITLE<br>SCHEMATIC DIAGRAM, SOCKET BOARD |  |
| MECH ENG<br>J. H. H. 1/8   |  | DATE<br>1/8 |  |                                                                   |  | SIZE<br>D                                |  |
| MFG ENG<br>J. H. H. 1/8    |  | DATE<br>1/8 |  |                                                                   |  | FSCM NO.<br>54193                        |  |
| QUAL ASSUR<br>J. H. H. 1/8 |  | DATE<br>1/8 |  |                                                                   |  | DRAWING NO.<br>30-701-0009               |  |
| APPROV<br>J. H. H. 1/8     |  | DATE<br>1/8 |  |                                                                   |  | SHEET 1 OF 1                             |  |



| REVISIONS |             |    |      |        |      |
|-----------|-------------|----|------|--------|------|
| LTR       | DESCRIPTION | DR | CHK  | APPR'D | DATE |
| A         | RELEASE     | SH | 4/10 | 4/10   | 4/10 |



- NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W, 5%, 10 OHMS.
  2. ALL CAPACITORS ARE IN MICROFARADS/50V.
  3. ALL DIODES ARE 1N4148.
  4. LAST REFERENCE DESIGNATORS USED: U8, R42, C25, CR18, Q17, J2.

|                           |  |              |                                                                     |  |                                         |
|---------------------------|--|--------------|---------------------------------------------------------------------|--|-----------------------------------------|
| DRAWN<br>SUENEE H         |  | DATE<br>8/84 | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES                 |  | <h1>DATA I/O</h1> <p>REDMOND, WASH.</p> |
| CHECKED<br>[Signature]    |  |              | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX .2<br>XXX .5<br>ANGULAR |  |                                         |
| ELEC ENG<br>[Signature]   |  |              | DO NOT SCALE DRAWING                                                |  | TITLE<br>SCHEMATIC<br>COMPONENT BOARD   |
| MECH ENG<br>[Signature]   |  |              |                                                                     |  | SIZE<br>D                               |
| MFG ENG<br>[Signature]    |  |              |                                                                     |  | FSM NO<br>54193                         |
| QUAL ASSUR<br>[Signature] |  |              |                                                                     |  | DRAWING NO<br>30-701-0152               |
| APPR<br>[Signature]       |  |              |                                                                     |  |                                         |



4

3

2

1

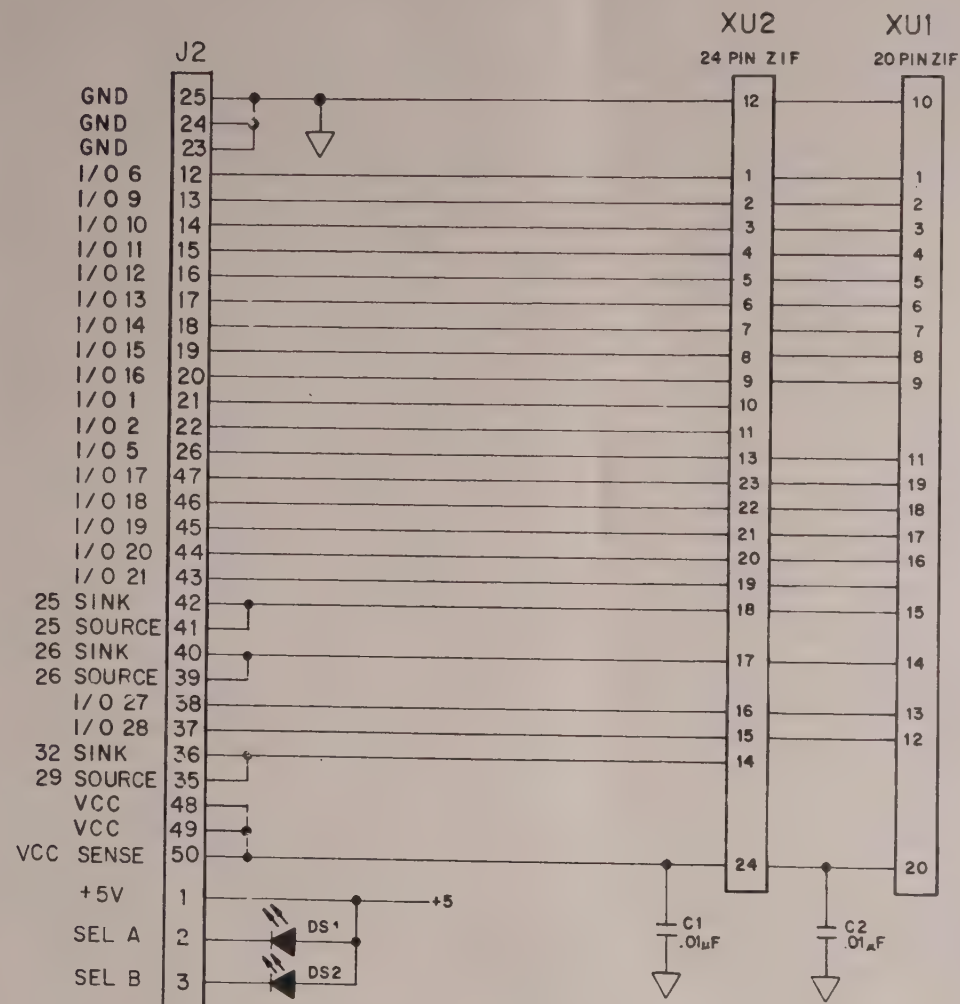
| REVISIONS |             |    |     |        |         |
|-----------|-------------|----|-----|--------|---------|
| LTR       | DESCRIPTION | DR | CHK | APPR'D | DATE    |
| A         | RELEASE     | SH | W   | W      | 10/1/84 |

D

C

B

A



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL CAPACITORS ARE IN MICROFARADS/50V.

2. LAST REFERENCE DESIGNATORS USED  
C2, XU2, J2, DS2

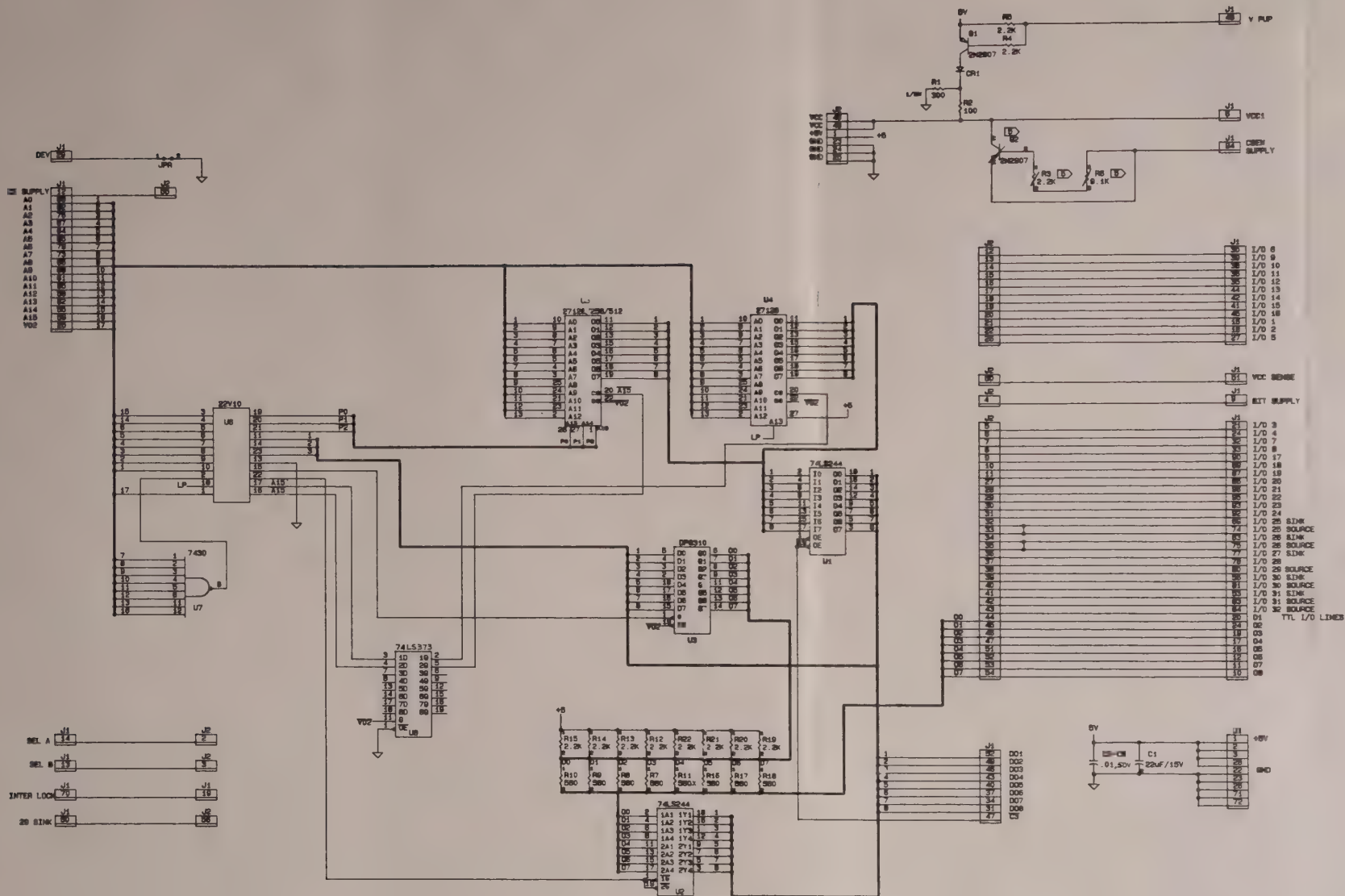
C

B

A

|             |      |                                                                   |      |                                    |           |
|-------------|------|-------------------------------------------------------------------|------|------------------------------------|-----------|
| APPROVALS:  |      | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES               |      | <b>DATA I/O</b> REDMOND, WASH      |           |
| DSN ENGR.   | DATE | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX .<br>XXX .<br>ANGULAR |      | TITLE SCHEMATIC,<br>DAUGHTER BOARD |           |
| MFG ENGR.   | DATE |                                                                   |      |                                    |           |
| QUAL ASSUR. | DATE | DRAWN BY                                                          | DATE | SIZE                               | CODE INCH |
| ENGR MGR.   | DATE | CHECKED BY                                                        | DATE | C                                  | 54193     |
| SCALE NONE  |      |                                                                   |      | DRAWING NO<br>30-701-0155          |           |
|             |      |                                                                   |      | SHEET 1 OF 1                       |           |





- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, OR
  2. ALL CAPACITORS ARE IN MICROFARADS.
  3. ALL DIODES ARE 1N4148
  4. LAST REFERENCE DESIGNATOR USED:

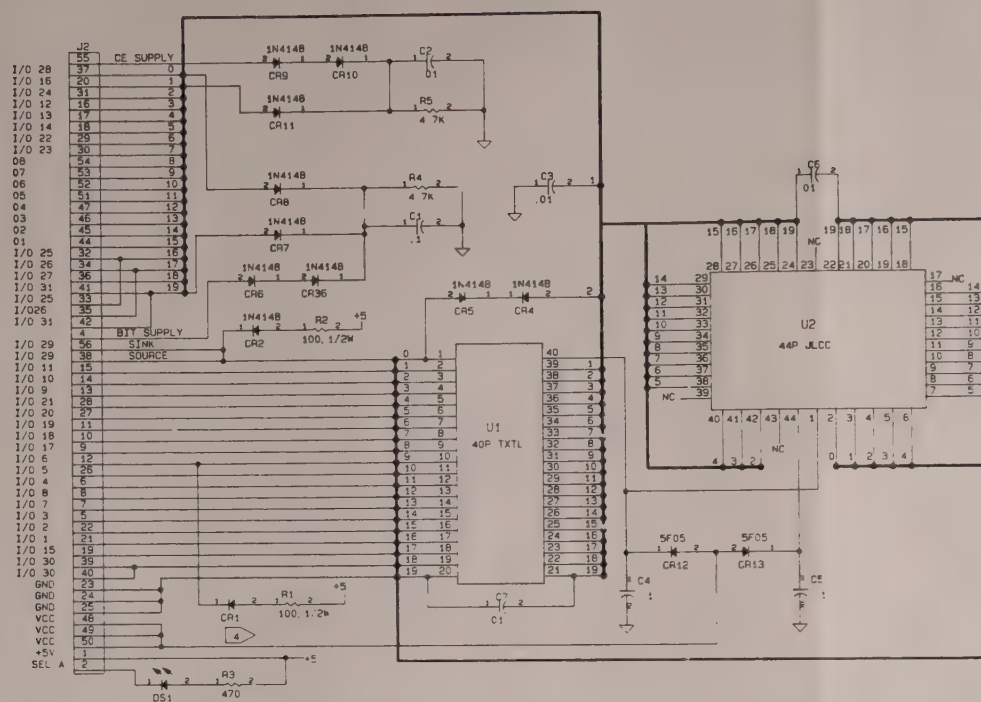
| REF            | DES. | ±5 | 4W/L |
|----------------|------|----|------|
| U1, U2, U3, U4 | 2C   | 10 |      |
| U5, U6         | 2B   | 14 |      |
| U7             | 2A   | 12 |      |
| U8             | 14   | 7  |      |

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SPECIFIC WRITTEN PERMISSION OF DATA I/O CORP.

|                      |  |                |  |                                                                     |  |                                             |  |
|----------------------|--|----------------|--|---------------------------------------------------------------------|--|---------------------------------------------|--|
| DRAWN<br>1/1/74      |  | DATE<br>1/1/74 |  | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES                 |  | <b>DATA I/O</b><br>REDMOND, WASH.           |  |
| CHECKED<br>1/1/74    |  | DATE<br>1/1/74 |  | TOLERANCES, UNLESS OTHERWISE SPECIFIED:<br>XX ±<br>XXX ±<br>ANGULAR |  |                                             |  |
| MECH ENG<br>1/1/74   |  | DATE<br>1/1/74 |  | DO NOT SCALE DRAWING                                                |  | TITLE<br>SCHEMATIC DIAGRAM,<br>MOTHER BOARD |  |
| MFG ENG<br>1/1/74    |  | DATE<br>1/1/74 |  | SIZE<br>D                                                           |  | FSCM NO<br>54193                            |  |
| QUAL ASSUR<br>1/1/74 |  | DATE<br>1/1/74 |  | DRAWING NO<br>30-701-2048                                           |  |                                             |  |
| APPROD<br>1/1/74     |  | DATE<br>1/1/74 |  |                                                                     |  |                                             |  |



| REVISIONS |                                        |    |               |        |      |
|-----------|----------------------------------------|----|---------------|--------|------|
| LTR       | DESCRIPTION                            | DR | CHK           | APPR'D | DATE |
| A         | RELEASE                                | SH | 13C           | CBD    | 66   |
| B         | INC ADDN A1, A2, PER<br>FCP #0295 1341 | LW | 87<br>5/27/87 | N      | 5 87 |



- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS.  
1/4W, 5%
  2. ALL CAPACITORS ARE IN MICROFARADS .50V
  3. LAST REFERENCE DESIGNATOR USED  
J2, C7, CR13, DS1, R5, U2

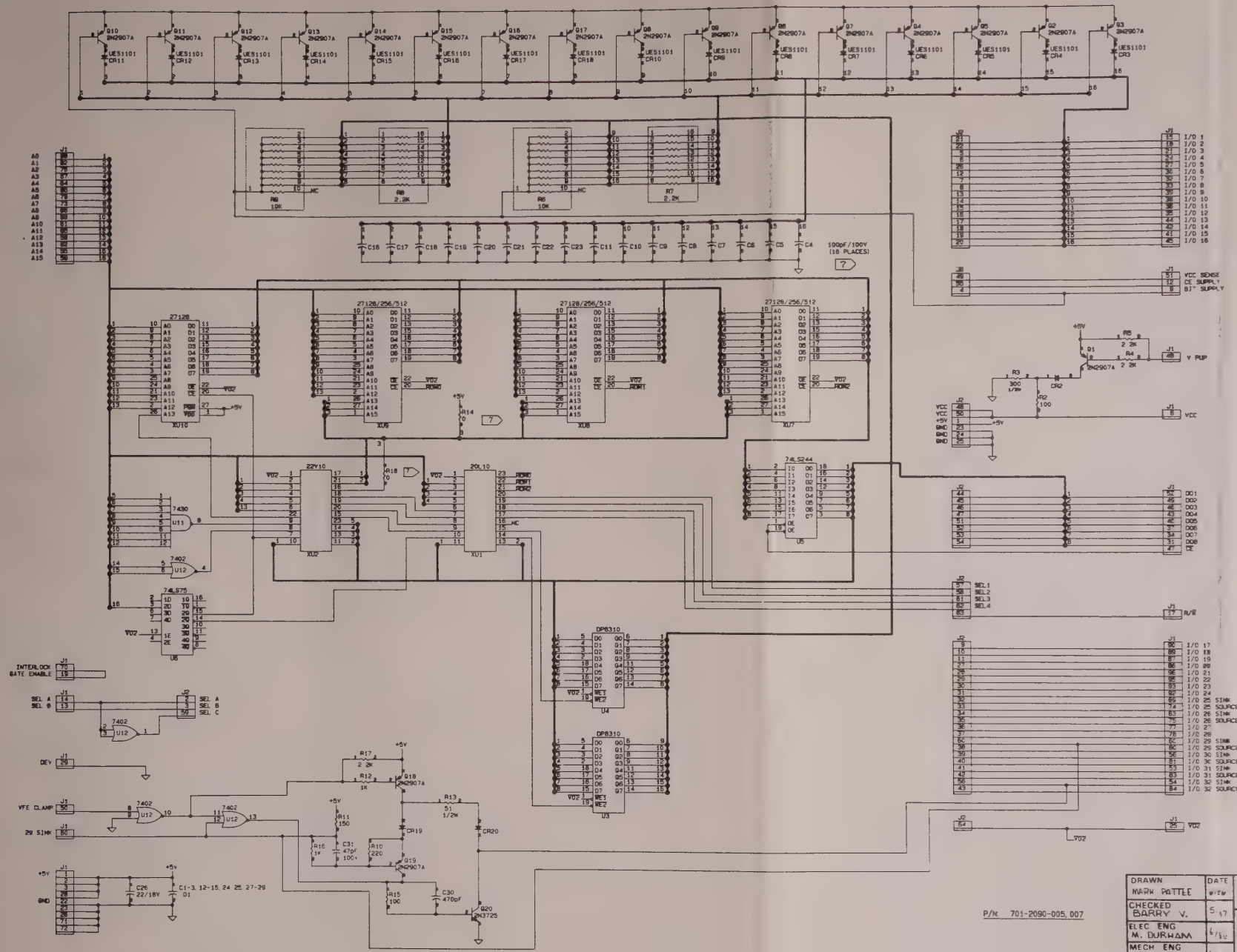
4 COMPONENTS OMITTED. CR1

P/N: 701-2045-003

|                           |  |                 |  |                                                                     |  |                                             |  |
|---------------------------|--|-----------------|--|---------------------------------------------------------------------|--|---------------------------------------------|--|
| DRAWN<br>JAMES V.         |  | DATE<br>5/2/87  |  | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES                 |  | <b>DATA I/O</b><br>REDMOND, WASH.           |  |
| CHECKED<br>JAMES V.       |  | DATE<br>5/2/87  |  | TOLERANCES, UNLESS OTHERWISE SPECIFIED:<br>.XX<br>.XXX ±<br>ANGULAR |  |                                             |  |
| ELEC ENG<br>J. MILLER     |  | DATE<br>1-10-86 |  | DO NOT SCALE DRAWING                                                |  | TITLE<br>I/O UNIT CIRCUIT<br>DAUGHTER BOARD |  |
| MECH ENG<br>C. BASSETT    |  | DATE<br>1-13-86 |  | SIZE<br>C                                                           |  | FSCM NO.<br>54193                           |  |
| MFG ENG<br>R. SHEPHERD    |  | DATE<br>1-13-86 |  | DRAWING NO.<br>31-100-1000                                          |  | SHEET 1 OF 1                                |  |
| QUAL ASSUR<br>M. FOLKERTS |  | DATE<br>1-13-86 |  | SCALE                                                               |  |                                             |  |
| APPRD<br>G. JAMES         |  | DATE<br>1/18/86 |  |                                                                     |  |                                             |  |



| REVIEWS |                            |    |     |        |
|---------|----------------------------|----|-----|--------|
| LTR     | DESCRIPTION                | DR | CHK | APPR'D |
| B       | REDRAWN W/O CHANGE         | VP | EV  | KM     |
| C       | INC. ADCN B1, PER ECP 0493 | VP | EV  | KM     |



NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. ALL RESISTORS ARE 1/4W, 5% AND IN OHMS  
 2. ALL CAPACITORS ARE .05V AND IN MICROFARADS  
 3. ALL DIODES ARE 1N4148  
 4. LAST REFERENCE DESIGNATOR USED:  
 U12: U2, C31, R18, C20, Q20  
 5. REFERENCE DESIGNATORS NOT USED:  
 R1, C41  
 6. POWER AND GROUND CHART

| REF             | DES | +5V | GND |
|-----------------|-----|-----|-----|
| U7, U8, U9, U10 | 20  | 14  |     |
| U1, U2          | 24  | 12  |     |
| U3, U4, U5      | 20  | 10  |     |
| U12, U13        | 14  | 7   |     |
| U6              | 5   | 12  |     |

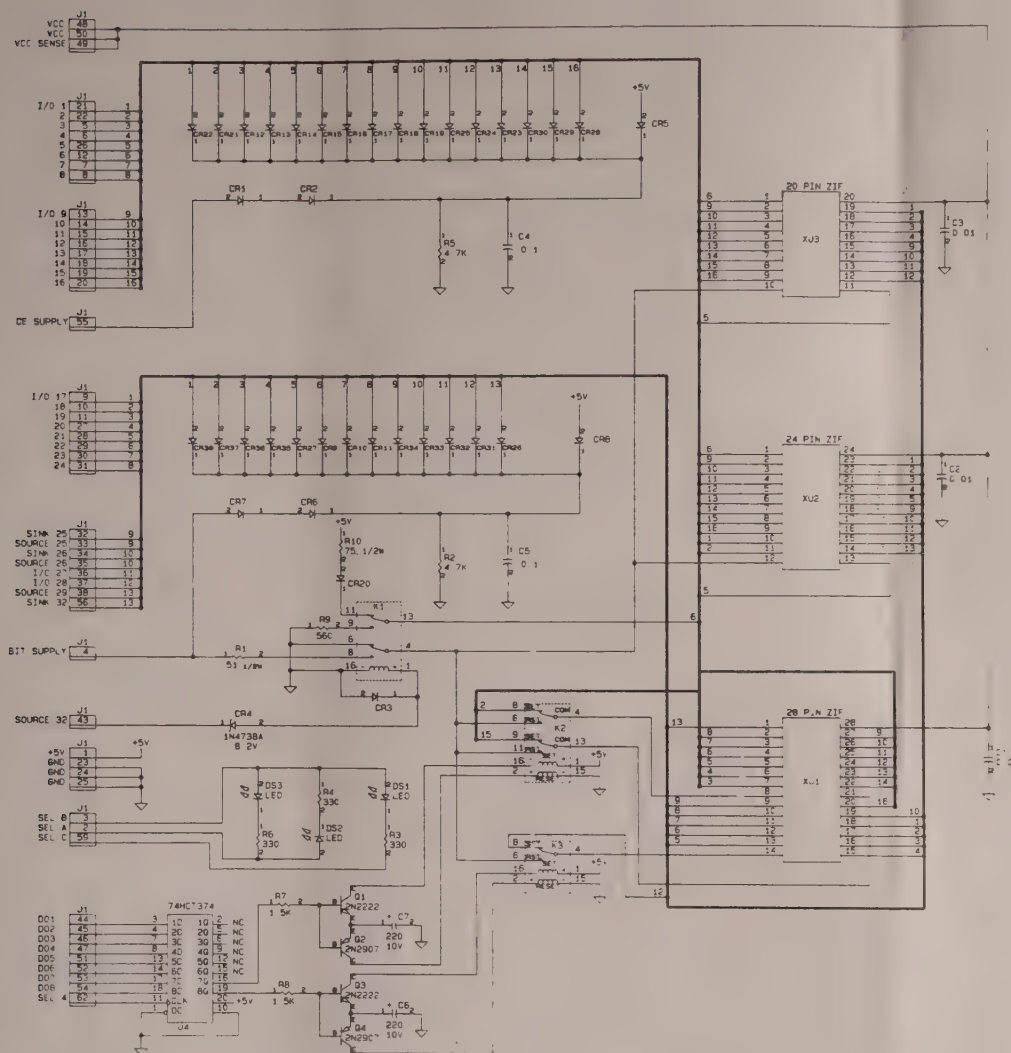
COMPONENTS OMITTED:  
 -D05, R18  
 -D07, R14, C4-11, 16-23

|                           |             |                                                                                       |                                                  |         |             |                      |
|---------------------------|-------------|---------------------------------------------------------------------------------------|--------------------------------------------------|---------|-------------|----------------------|
| DRAWN<br>MARK PATTEE      | DATE<br>5/7 | UNLESS OTHERWISE<br>SPECIFIED DIMENSIONS<br>ARE IN INCHES                             | <b>DATA I/O</b><br>REDMOND, WASH.                |         |             |                      |
| CHECKED<br>BARRY V.       | 5/17        | TOLERANCES UNLESS<br>OTHERWISE SPECIFIED<br>XX ±<br>XXX ±<br>ANGULAR                  | TITLE SCHEMATIC DIAGRAM,<br>GENERIC MOTHER BOARD |         |             |                      |
| ELEC ENG<br>M. DURHAM     | 6/30        |  | SIZE                                             | FSCM NO | DRAWING NO  |                      |
| MECH ENG<br>B. REGESTER   | 5/11        |                                                                                       | <b>D</b>                                         | 54193   | 30-701-2090 |                      |
| MFG ENG<br>R. SHEPHERD    | 4/30        |                                                                                       |                                                  |         |             | DO NOT SCALE DRAWING |
| QUAL ASSUR<br>M. FOLKERTS | 5/10        |                                                                                       |                                                  |         |             |                      |
| APPD                      | 5/1         |                                                                                       |                                                  |         |             |                      |

P/N 701-2090-005.007



| LTR |  | DESCRIPTION | DR | CHK | APPR'D  | DATE |
|-----|--|-------------|----|-----|---------|------|
| A   |  | RELEASE     | MC | BY  | 11/4/61 | 6/86 |



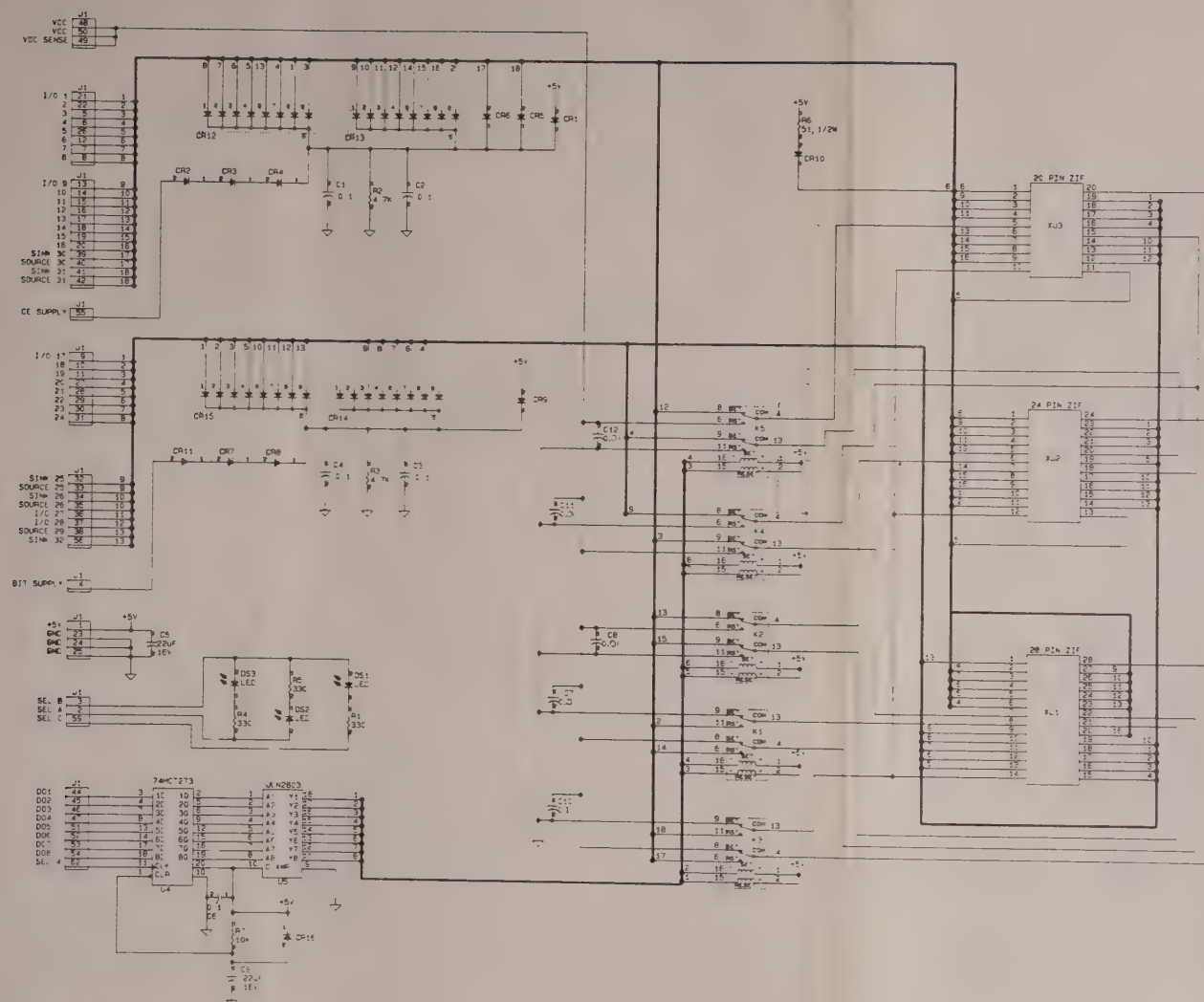
- NOTES, UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS
  2. ALL CAPACITORS ARE IN MICROFARADS 50V
  3. ALL DIODES ARE 1N4148
  4. LAST REFERENCE DESIGNATOR USED

P/N 701-2091-001

|                                                       |  |                      |                                                                   |                                                  |                                 |
|-------------------------------------------------------|--|----------------------|-------------------------------------------------------------------|--------------------------------------------------|---------------------------------|
| DRAWN<br>MAG. FATTEN                                  |  | DATE<br>E RE         | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES               |                                                  | <b>DATA I/O</b><br>REMOUNT WASH |
| CHECKED<br>B. Velders                                 |  | DATE<br>11/4/61      | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX ±<br>XXX ±<br>ANGULAR |                                                  |                                 |
| ELEC ENG<br>MECH ENG<br>MFG ENG<br>QUAL ASSUR<br>APPD |  | DO NOT SCALE DRAWING |                                                                   | TITLE<br>SCHEMATIC DIAGRAM<br>DIP DAUGHTER BOARD |                                 |
| SIZE<br>D                                             |  | FSCM NO<br>54193     |                                                                   | DRAWING NO<br>30-701-2091                        |                                 |
| SCALE<br>NONE                                         |  | SHEET<br>1 OF 1      |                                                                   |                                                  |                                 |



| REVISIONS |             |    |        |             |
|-----------|-------------|----|--------|-------------|
| LTR       | DESCRIPTION | DR | CHK    | APPR'D DATE |
| A         | RELEASE     | MD | 8/1/87 | 8/9/87      |



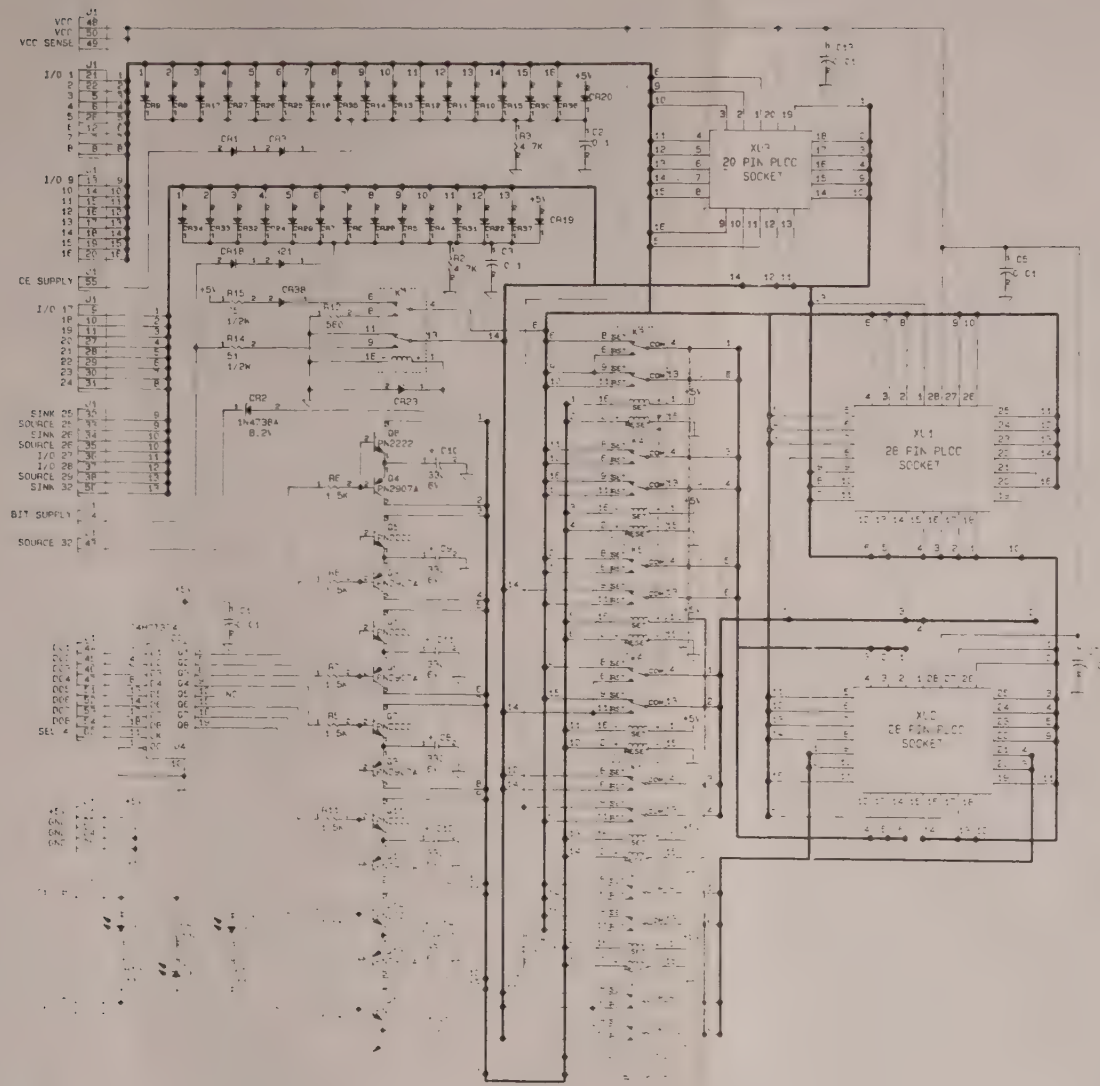
- NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. ALL RESISTORS ARE IN OHMS  
 2. 1/4 W  
 3. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED  
 4. ALL DIODES ARE 1N4148  
 5. ALL REFERENCE DESIGNATORS USED  
 6. 0.01 OHM 0.5% 1/4 W 0.1% AT #1

P/N 701-2138-001

|                                  |  |                                 |  |                                                                 |  |                                                           |  |
|----------------------------------|--|---------------------------------|--|-----------------------------------------------------------------|--|-----------------------------------------------------------|--|
| DRAWN<br>MAY PATTEG<br>1/87      |  | DATE<br>1/87                    |  | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES             |  | REVISIONS                                                 |  |
| CHECKED<br>B. Veldura<br>2/6/87  |  | ELEC ENG<br>2/6/87              |  | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX<br>XXX ±<br>ANGULAR |  | TITLE<br>SCHEMATIC DIAGRAM,<br>GENERIC DIP DAUGHTER BOARD |  |
| MECH ENG<br>B. Foster<br>2/6/87  |  | MFG ENG<br>M. Veldura<br>2/6/87 |  | DO NOT SCALE DRAWING                                            |  | SIZE<br>D                                                 |  |
| QUAL ASSUR<br>P. D. S.<br>2/6/87 |  | APPR'D<br>K. Veldura<br>2/6/87  |  | FSCM NO<br>54193                                                |  | DRAWING NO<br>30-701-2138                                 |  |
| SCALE: 1/4" = 1"                 |  | Dwg No.                         |  | Rev                                                             |  | Date                                                      |  |



| LTR | DESCRIPTION                | DR | CHK | APPR'D | DATE |
|-----|----------------------------|----|-----|--------|------|
| 2   | RELEASE                    | MP | BV  | K.M.   | 7-86 |
| 3   | INC ADJN AT PER ECP # 0309 | LW | BN  | K.N.   | 5-87 |



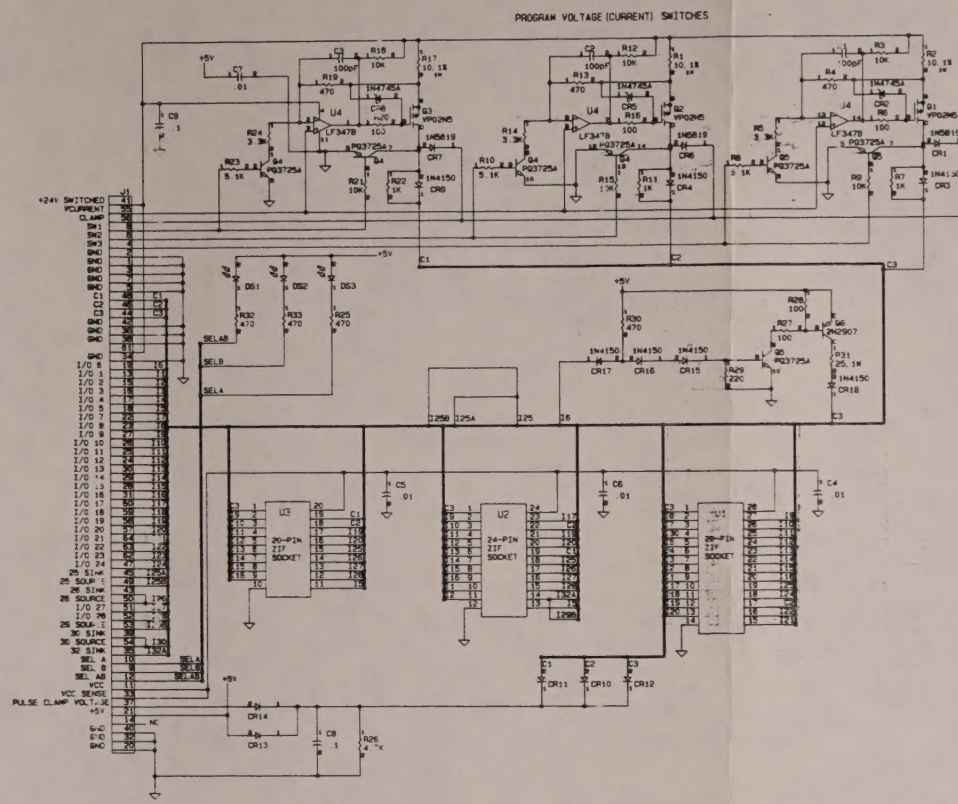
|                          |              |                                                                   |                                                   |                  |
|--------------------------|--------------|-------------------------------------------------------------------|---------------------------------------------------|------------------|
| DRAWN<br>M. MILLER       | DATE<br>7/10 | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES               | <b>DATA I/O</b>                                   |                  |
| CHECKED<br>M. MILLER     | 7/10         | TOLERANCES UNLESS OTHERWISE SPECIFIED<br>XX ±<br>XXX ±<br>ANGULAR | TITLE<br>SUMMATIC DATA I/O<br>SHEETED MATHEMATICS |                  |
| ELEC ENG<br>T. CYLINDER  | 7/10         | DO NOT SCALE DRAWING                                              | SIZE<br><b>D</b>                                  | FSCM NO<br>54193 |
| MECH ENG<br>M. HOGSTON   | 7/10         |                                                                   | DRAWING NO<br>3                                   |                  |
| MFG ENG<br>N. SHEPHERD   | 7/10         |                                                                   |                                                   |                  |
| QUAL ASSUR<br>M. TOLKATE | 7/10         |                                                                   |                                                   |                  |
| APPD<br>M. MILLER        | 7/10         |                                                                   |                                                   |                  |
| SCALE                    |              | SHEET 1 OF 1                                                      |                                                   |                  |







| LTR | DESCRIPTION | DR        | CHK       | APPR'D     | DATE   |
|-----|-------------|-----------|-----------|------------|--------|
| A   | RELEASE     | <i>JK</i> | <i>RL</i> | <i>KIM</i> | 2-9-69 |



- NOTES:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
  2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
  3. ALL DIODES ARE 1N4148.
  4. LAST REFERENCE DESIGNATOR USED: CR, CR18, R33, Q6, U4, J1, DS3.

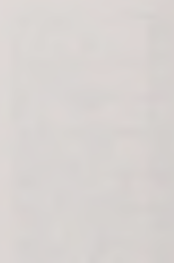
P/N 30-701-2104-001

|                                |  |                |                                                                    |  |                                                       |
|--------------------------------|--|----------------|--------------------------------------------------------------------|--|-------------------------------------------------------|
| DRAWN<br>SH / JK               |  | DATE<br>2/5/69 | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES                |  | <b>DATA I/O</b><br>REDMOND, WASH.                     |
| CHECKED<br><i>Ed Roster</i>    |  | DATE<br>1/9/71 | TOLERANCES, UNLESS OTHERWISE SPECIFIED<br>XX ±<br>XXX ±<br>ANGULAR |  |                                                       |
| ELEC ENG<br><i>Ed Roster</i>   |  | DATE<br>1/1/71 | DO NOT SCALE DRAWING                                               |  | TITLE<br>SCHEMATIC DIAGRAM<br>AIM P/T ADPT SOCKET BD. |
| MECH ENG<br><i>Boyd</i>        |  | DATE<br>1/1/71 | SIZE<br><b>D</b>                                                   |  | FSCM NO<br>54193                                      |
| MFG ENG<br><i>Ed Roster</i>    |  | DATE<br>1/1/71 | DRAWING NO<br>30-701-2104                                          |  | SCALE<br>D. A. D.                                     |
| QUAL ASSUR<br><i>Ed Roster</i> |  | DATE<br>1/1/71 | SHEET 1 OF 1                                                       |  |                                                       |

PLATE 100



PLATE 101





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